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EMR HATBORO

1410 FREQUENCY RESPONSE ANALYZER

INSTRUCTION MANUAL

EMR DIVISION OF WESTON INSTRUMENTS, INC · A SCHLUMBERGER COMPANY

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PARTS TO BE SHIPPED WITH STANDARD 1410 (AND AR OPTION)

QTY.	EMR PART NO.	ITEM
1	---	1410 Frequency Response Analyzer
1	014-3-20-001	Power Cord
2	881-3-01-048	Rack Mount Ears (T-Bars)
1	881-5-01-253	Extender Board
2	---	1410 Manual

PARTS TO BE SHIPPED WITH F OPTION 1410

1	---	1410 Frequency Response Analyzer
1	014-3-20-001	Power Cord
2	881-3-01-048	Rack Mount Ears (T-Bars)
1	881-5-01-253	Extender Board
2	---	1410 Manual
1	023-3-29-007	Elco Connector #00-8016-056-217-704
1	023-3-29-006	Elco Connector #00-8016-020-217-704

A

Rev.
1. DRN00514
ff

Note: For revisions see marked prints

FIRST RELEASE-DRN 00461

1410 SHIPPING LIST

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1 - GENERAL INFORMATION

1.1 - Introduction

The Model 1410 Frequency Response Analyzer measures phase and amplitude over a frequency range of .001 Hz to 10K Hz. It consists of a Function Generator to stimulate the device under test, a Correlator to analyze the return signal, and a Display to indicate the results of the measurement in polar coordinates.

1.2 - Instrument Description

The Model 1410 Frequency Response Analyzer is all solid state construction and employs the use of DTL (Diode Transistor Logic), and TTL (Transistor Transistor Logic) Integrated Circuits, as well as Integrated Circuit Amplifiers. The internal analog switching is accomplished by the use of FET (Field Effect Transistors) and a tuning fork oscillator is used for the correlator time standard. The frame is of welded steel construction for ruggedness and an exhaust fan is provided for maintaining an even distribution of temperature inside the case. A result of these features is an instrument which is mechanically rugged with a high degree of temperature stability and low power consumption.

1.3 - Options

The following options are available in the Model 1410 Frequency Response Analyzer:

AR- Auto Ranging of the correlator input range.

F - Programmable for remote operation.

Note: The F Option includes the AR Option.

1.4 - Instrument Identification

A name plate located on the rear panel of the instrument contains the model and serial numbers of the instruments.

1.5 - SPECIFICATIONS - MODEL 1410

1.5.1 - FUNCTION GENERATOR

Frequency

Range: 0.001 Hz-9990 Hz

Accuracy: 0.5% of selected frequency

Output Waveforms

Sinusoidal, Square, Suppressed Carrier

Harmonic Distortion

No component greater than 0.5% F.S. to 999 Hz
2.0% F.S. to 9990 Hz

Output

Ranges: 0-1.5 volts peak, 0-15 volts peak

Stability: 0.1% Short Term, 0.5% Long Term

Impedance: Less than 1 ohm

Control: Potentiometer

Power: 5 mA at Full Output

DC Content: 0.25% F.S., adjustable to zero

Carrier Input

Level: 10 volts to 115 volts rms

Frequency: DC to 10 kHz

Carrier Phase Shift: Less than 1° to 10 kHz

1.5.2 - CORRELATOR

Return Signal

Input: Balanced

Full Scale Ranges: 150 mV, 1.5V, 15V, 150 V

Input Impedance: 150 mV Range - 100K
All other ranges - 1M

Noise & Harmonic Rejection: > 40 db

DC Rejection: 100% F.S. adjustable to ±100 volts

Form of Display: Dual readout - amplitude (R) and phase (θ)

Accuracy: (.001 Hz to 1 kHz)

Ampl: ±1% of reading or 0.3% of F.S. whichever is greater, ±1 LSD

Phase: ±1/2° at F.S. (amplitude), linearly degraded to ±1° at 0.1 F.S., ±1 LSD

Accuracy: (1 kHz to 9990 Hz)

Ampl: ±1.5% of reading or 0.5% of F.S. whichever is greater, ±1 LSD

Phase: ±3/4° at F.S., linearly degraded to ±1.5° at 0.1 F.S., ±1 LSD

Measurement Time

.001 to 1 Hz - 1 1/2 cycles of test frequency +1 second max.

1 Hz to 9990 Hz - 2 seconds max.)

Demodulator

Frequency: 0 to 10 kHz

DC Digital Voltmeter

±1% of F.S.

1.5.3 - POWER REQUIREMENTS AND PHYSICAL DATA

Power Required

Voltage: 115 V or 230 V rms

Frequency: 50-400 Hz

Consumption: Less than 120 watts

Componentry

All Silicon - DTL I/C's

Packaging

Dimensions: 7" H x 19" W x 18" D

Weight: Approximately 38 lbs.

2 - INSTALLATION

2.1 - Incoming Inspection

This instrument was carefully inspected mechanically and electrically before shipment. It should be physically free of marrs or scratches and in perfect electrical order upon receipt. To confirm this, the instrument should be inspected for physical damage in transit. Also, check for supplied accessories and test the electrical performance of the instrument using the procedure outlined in the performance verification section of the manual. If there is damage or a deficiency, contact the factory immediately.

2.2 - Installation

Once it has been established that the unit is free of damage in shipment it is ready for operation. Connect the power cable supplied with the instrument and check for proper power source requirements.

2.3 - Power Source Requirements

The Model 1410 can be operated from a 115 or 230 V, 50 to 400 Hz AC source. Primary power requirements are set by the rear panel line voltage switch. Before plugging the Model 1410 into the power source, check that the designation of the two position line voltage switch matches the line voltage of the power source and that the proper fuse is installed.

2.4 - Three Conductor Power Cable

To protect operating personnel, National Electrical Manufacturers Association (NEMA) recommends that the instrument panel and cabinet be grounded. The Model 1410 is equipped with a detachable three conductor power cable which, when plugged into the proper receptacle, grounds the instrument. The round offset pin on the power cable conductor is the ground connection. To retain the protection feature when operating the instrument from a two contact outlet, use a three conductor to 2 conductor adapter and connect the adapter wire to a suitable ground.

2.5 - Rack or Bench Mount Consideration

The Model 1410 Frequency Response Analyzer is shipped with plastic feet in place ready for use as a bench instrument. However, the modular instrument enclosure system enables easy conversion from bench to rack model and vice versa. Conversion to rack mount is accomplished by removing the plastic feet and replacing the angle pieces at both sides of the front panel with the rack adapter pieces. The rack mount for the instrument is an EIA standard width of 19". When rack mounted in a rack using mounting flanges, additional support at the rear of the instrument should be provided if vibration or similar stress is likely.

2.6 - Repacking for Shipment

The following is a general rule for repackaging an instrument for shipment. If you have any questions contact the factory or local sales representative. Note: If the instrument is to be shipped to the factory for service or repair, attach a tag to the instrument identifying the owner and indicating the service or repair to be accomplished. Include the model number and full serial number of the instrument. In any correspondence, identify the instrument by model number and serial number.

A) Place the instrument in the original container if available. If the original container is not available, a suitable container can be purchased from the factory.

If the original container is not used:

B) Wrap the instrument in heavy paper or plastic before placing it in an inner container.

C) Use a substantial quantity of packing material around all sides of the instrument and protect the panel faces with cardboard strips.

D) Place the instrument in an inner container in a heavy carton or wooden box and seal with strong tape or metal bands.

E) Mark shipping container with:

"DELICATE INSTRUMENT"

"FRAGILE", etc.

2.7 - Identification of Rear Panel Connectors for Options

J101 - (Option F) Generator Output, Type BNC. (In parallel with front panel output).

J102 - (Option F) Carrier Input, Type BNC. (In parallel with front panel carrier input).

J103 - (Option F) Hi Correlator Input, Type BNC. (In parallel with front panel Hi Correlator input).

J104 - (Option F) Lo Correlator input, Type BNC. (In parallel with front panel Lo Correlator input).

J105 - (Option F) Output Logic, Type ELCO #00-8016-056-000-707 Mating connector #00-8016-056-217-704 (remote readout of amplitude and phase shift of resultant and frequency programmed).

J106 - (Option F) Input Logic, Type ELCO #00-8016-056-000-707 Mating Connector #00-8016-056-217-704 (inputs for remote programming data).

J107 - (Option F) Aux. Output Logic, Type ELCO #00-8016-020-000-707 Mating Connector #00-8016-020-217-704.

2.8 - J105 connector pin designations for remote readout are described on "Output Signal Chart" Fig. 2.1.

2.9 - J106 connector pin designations for remote programming are described in "Input Signal Chart" Fig. 2.2.

2.10 - J107 connector pin designations for remote programming are described in "Aux. Output Chart" Fig. 2.3.

FIGURE 2.1

OUTPUT SIGNAL CHART

PIN		FUNCTION		
J105 -	A	.1°	Phase	
	B	.2°	Phase	
	C	.4°	Phase	
	D	.8°	Phase	
	E	1°	Phase	
	F	2°	Phase	
	H	4°	Phase	
	J	8°	Phase	
	K	10°	Phase	
	L	20°	Phase	
	M	40°	Phase	
	N	80°	Phase	
	P	100°	Phase	
	R	Phase	Lead-Lag (Lead is true state)	
	S	1R	Amplitude	
	T	2R	Amplitude	
	U	4R	Amplitude	Amplitude is Linear for "Lin R" Measurements
	V	8R	Amplitude	
	W	10R	Amplitude	Amplitude is Logrithmic for "Log R" Measurements
	X	20R	Amplitude	
	Y	40R	Amplitude	
	Z	80R	Amplitude	
	$\overline{A}$	100R	Amplitude	
	$\overline{B}$	200R	Amplitude	
	$\overline{C}$	400 R	Amplitude	
	$\overline{D}$	800R	Amplitude	
	$\overline{E}$	1000 R	Amplitude	
	$\overline{F}$	1 - Decimal PT	(BCD Code of Decimal Places to the Left)	

$\overline{H}$	2 - Decimal PT	
$\overline{J}$	4 - Decimal PT	
$\overline{K}$	MEASURE COMPLETE	
$\overline{L}$	$\overline{\text{MEASURE COMPLETE}}$ (complement)	
$\overline{M}$	$\overline{\text{MEASURE COMPLETE AND IN RANGE}}$ (complement)	
$\overline{N}$	MEASURE COMPLETE AND IN RANGE	
$\overline{P}$	10F	Frequency Programmed
$\overline{R}$	20F	Frequency Programmed
$\overline{S}$	40F	Frequency Programmed
$\overline{T}$	80F	Frequency Programmed
$\overline{U}$	100F	Frequency Programmed
$\overline{V}$	200F	Frequency Programmed
$\overline{W}$	400F	Frequency Programmed
$\overline{X}$	800F	Frequency Programmed
$\overline{Y}$	1000F	Frequency Programmed
$\overline{Z}$	2000F	Frequency Programmed
AA	4000F	Frequency Programmed
BB	8000	Frequency Programmed
CC	10^{-0}	Frequency Programmed
DD	10^{-1}	Frequency Programmed
EE	10^{-2}	Frequency Programmed
FF	10^{-3}	Frequency Programmed
	(10^{-4} is true when CC, DD, EE, and FF are all false)	
HH	$\overline{\text{Input Overload}}$	
JJ	SPARE	
KK	SPARE	
LL	SPARE	
MM	GND	
NN	GND	

FIGURE 2.2

INPUT SIGNAL CHART

PIN		FUNCTION	
J106 -	A	10F	Frequency Programming
	B	20F	Frequency Programming
	C	40F	Frequency Programming
	D	80F	Frequency Programming
	E	STROBE	
	F	100F	Frequency Programming
	H	200F	Frequency Programming
	J	400F	Frequency Programming
	K	800F	Frequency Programming
	L	STROBE	
	M	1000F	Frequency Programming
	N	2000F	Frequency Programming
	P	4000F	Frequency Programming
	R	8000F	Frequency Programming
	S	STROBE	
	T	10^{-0}	Frequency Programming
	U	10^{-1}	Frequency Programming
	V	10^{-2}	Frequency Programming
	W	10^{-3}	Frequency Programming
		10^{-4}	(True when T, U, V, and W are false)
	X	STROBE	
	Y	Demod IN-OUT ("IN" is true command)	
	Z	AC-DC (AC is true command)	

$\overline{A}$	∿ - ⊓ (⊓ is true command)	
$\overline{B}$	STROBE	
$\overline{C}$	Stop at 0°	
$\overline{D}$	Stop at 90°	
$\overline{E}$	0° - 180° Phase (180° is true command)	
$\overline{F}$	STROBE	
$\overline{H}$	.1V	Amplitude Programming
$\overline{J}$	.2V	Amplitude Programming
$\overline{K}$	.4V	Amplitude Programming
$\overline{L}$	.8V	Amplitude Programming
$\overline{M}$	STROBE	
$\overline{N}$	1V	Amplitude Programming
$\overline{P}$	2V	Amplitude Programming
$\overline{R}$	4V	Amplitude Programming
$\overline{S}$	8V	Amplitude Programming
$\overline{T}$	STROBE	
$\overline{U}$	10V	Amplitude Programming
$\overline{V}$	STROBE	
$\overline{W}$	X10 INT	
$\overline{X}$	1.5V - 15V PEAK AMPLITUDE (1.5V is true command)	
FF	R and θ - Calibrate is true command	
$\overline{Y}$	STROBE	

$\overline{Z}$	150.0V range
AA	15.V range
BB	0.15V range
CC	Auto Range
	(1.5V range true if $\overline{Z}$, AA, BB and CC are all false)
DD	STROBE
EE	Measure Command (true pulse for single measurement, true level for continuous measurement) (for single measurement pulse must be between 300 μ sec. and 1 sec. in width) (not strobed).
MM	+5 volts for programming
NN	Circuit Common for Programming

FIGURE 2.3

AUX. OUTPUT SIGNAL CHART

PIN		FUNCTION	
J107 -	A	Input Overload	(Twisted)
	B	GND Return	(Pair)
	C	Measure Complete and In Range	(Twisted)
	D	GND Return	(Pair)
	E	Measure Complete	(Twisted)
	F	GND Return	(Pair)
	H	Out of Range	(Twisted)
	J	GND Return	(Pair)
	K		
	L		
	M		
	N		
	P		
	R		
	S		
	T		
	U		
	V		
	W		
	X		

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3 - OPERATING INSTRUCTIONS

3.1 - General

3,1.1 - The EMR frequency response analyzer will measure the amplitude and phase of a signal from a unit under test which is being stimulated by the generator. The amplitude is measured in peak volts from 150 mv full scale, to 150 v full scale, in four ranges. Phase is measured from 0 to 179.9° - lead or lag with 0.1° resolution.

3.2 - Front Panel and Controls Description

3.2.1 - The Front panel is arranged in three general sections. The controls to the right of center being for selection of function generator test conditions. The controls to the left of center being for correlator test conditions, and the upper portion being the display of the results.

3.3 - Rear Panel Description

3.3.1 - The rear panel is divided into two parts. The left side, when viewed from the rear, contains the power input connector, fuse holder, and a slide switch to change the instruments power requirement from 115 V to 230 V. CAUTION: Be certain the correct fuse is installed for the operating voltage selected.

3.4 - Instrument Operation

3.4.1 - In order that maximum utilization of the instruments flexibility may be employed each function will be discussed as it relates to the entire instrument.

3.4.2 - Function Switch

AC-DC: In order to better understand the operation of this switch, think of the generator section as being a modulator. In the DC position the instrument will modulate an internal DC reference with a sine wave of the frequency and amplitude selected. In the AC position it will modulate the reference which is inserted at the carrier input jack in the lower center of the front panel. This feature enables the use of a suppressed carrier (or balanced) modulated signal for excitation of AC systems. Modulation is always 100%.

∿-⊓: The output wave form will be a sine wave or square wave, de - pending on the position of this switch. The square wave function is an added feature of the generator section only and would not normally be used as a stimulus when frequency response is being measured by the correlator section. But when it is used, it must be remembered that the correlator only measures the fundamental frequency component of the return signal.

3.4.3 - STOP Switch

This switch has a center off position for normal operation of the generator section. The 0° position, when actuated, will stop the output waveform at a level equivalent to 0°, however, this 0° position will be offset by the weighting factor of 1/2°. In other words if the phase switch were actuated alternately between 0 and 180°; the output at the generator output terminals would be of a magnitude equal to the sine of 1/2° times the peak amplitude setting. When actuated in the 90° position, the output waveform will be the peak amplitude of the sine wave. If the phase switch is alternately actuated between the 0 - 180° position the output level will be representative of the positive and negative peaks of the sine wave respectively. This switch is very useful when operating electro mechanical systems where pre-positioning of the extreme limits of travel would be desirable before setting up the conditions of the test. Note: If this switch is actuated at a very low frequency, time will have to be allowed for the instrument to continue from the point on the waveform at the time the switch is actuated to the position commanded by the actuation of the switch. This amount of time could be as much as 1/40th of the time required for one cycle of the test frequency set on the frequency switch.

3.4.4 - BIAS Switch and LEVEL Adjust

This control is used to offset the output waveform with a DC level from 0 to ±10 volts and is used as follows: The switch has a center off position for normal operation and a positive and negative position for the appropriate polarity of offset desired. Actuate the switch to the desired polarity and adjust the ten turn dial to the desired amplitude of the DC offset. The generator output is limited to 15 V peak. Therefore, any DC offset selected by this feature, when combined with the peak amplitude must add up to less than 15 v peak. For example, if a 10 volt offset is desired, then the maximum peak amplitude of the sine wave selected can not exceed 5 volts. This function is also affected by the position of the amplitude range switch which will be discussed in the paragraph pertaining to amplitude setting (3.4.6)

3.4.5 - Phase Switch

This switch has two positions and provides for 180° phase shift in the output signal relative to the correlator operation. It is useful when measuring inverted signals so that it will not be necessary to subtract 180° from all phase angle readings.

3.4.6 - Amplitude range switch and level control

When the amplitude switch is placed in the 15 volt position the level adjust potentiometer is adjustable from 0 to 15 V peak output. When in the

0 to 1.5 volt position it provides for a 10 to 1 higher resolution of the amplitude level set potentiometer. The 0 to 1.5 volt range also increases the resolution of the bias control such that its range is 0 to 1 volt rather than 0 to 10 volts.

3.4.7 - Zero Adj (Generator)

This screw driver adjustment, which is immediately below the output level adjustment potentiometer, is used to adjust out any residual DC offset present in the generator output. Before adjusting this, be certain that the bias control is not introducing any DC to the output terminals. Its purpose is to adjust out any long term drift of the output amplifier without requiring recalibration.

3.4.8 - Generator Output Terminals

These terminals are connected as follows: The terminal farthest to the right is connected to the chassis and to the ground pin of the power cord. The center terminal marked Signal Ground is connected to the internal circuit common. These two jacks are linked together with an external shorting link which can be removed for floating operation where the chassis ground must be connected with other grounds to prevent noise pick up. The red terminal marked "Output" is the generator output.

CAUTION: In order to maintain very low output impedance of the generator the output amplifier is connected directly to these output jacks and care MUST be taken to avoid connection of these terminals to a low impedance power source as damage to the output amplifier could result.

3.4.9 - Frequency Select Switch

This switch consists of three binary coded decimal switches on the left with a fixed 0 in the least significant position. On the right there is a five position multiplier switch with numerals 0 through 4. These numbers represent the negative exponent of ten to which the frequency selected is raised. When the frequency switch is in the position that reads 9990 and the multiplier switch position to read 10^{-0}, then the frequency would be 9,990 Hz which is the maximum frequency. It can be seen that a mid range frequency, such as 1 Hz could be derived in one of several ways, for example, you could have 0010 $X10^{-1}$ or 1000 $X10^{-3}$ either of which is an acceptable way of setting the frequency.

3.4.10 - Carrier Input

The carrier input is a BNC connector located in the center of the front panel. Input levels of 10-115 V RMS are provided by use of the level adjust potentiometer located directly over the input jack.

3.4.11 - Integration Switch

This switch has two positions, X1 for a normal measurement and X10 for a ten times integration period. When the switch is in the X1 position, the period of analysis will be one second plus the completion of the cycle of test signal. For example, 0.5 Hz has a period of 2 seconds, so at the one second time, analysis would be half way through and would complete itself on the completion of that one cycle of test signal. This would be followed by a computation time which can vary from 50 ms to 1 second depending on the phase angle and amplitude. So the maximum measurement time for 0.5 Hz to 9990 Hz would be three seconds at the low end and a maximum of 2 seconds at the high end. For frequencies below 0.5 Hz, it would be one complete cycle of the test frequency plus the one second computation time.

Example: At the lowest frequency of .001 Hz, the measurement time would be 16 minutes plus 1 second. Additional time amounting to as much as one half cycle of test frequency is necessary prior to the analysis time for synchronization of the correlator to the generator. This means if the measure command were actuated just after a zero crossing occured, a half cycle would be necessary before synchronization could occur; therefore, the .001 Hz measurement could be a maximum of 8 minutes for the half cycle to synchronization 16 minutes for the cycle of test signal and one second for the computation.

Since noise rejection is dependent on the number of cycles of test signal being analyzed the X10 position is provided to improve noise rejection when a noise frequency is present which is close to the test frequency. For frequencies below 0.5 Hz it would simply be 10 periods. There is some degradation of accuracy when using the X10 integration; however, the added noise rejection, when needed, far outweighs the slight degradation of accuracy.

3.4.12 - Lead Switch

This switch has three positions; Center Off, 45° Lead or 90° Lead. The center off position is for normal operation. The other two positions are provided for a self test of the instrument. When in the center position and a measure command actuated, the correlator is synchronized to start and stop at zero crossings of the test signal. In the 45° position, synchronization occurs at the 45° point and stops at the 45° point, thereby introducing a 45° lead in the answer. The same is true for the 90° position, except for the magnitude of the phase angle. These test positions can be used when operating in either the R - θ or CAL Position of the mode switch.

3.4. 13 - Demodulator Switch

This switch has two positions, IN and OUT. It is independent of the AC or DC mode of the generator but shares the same carrier reference which is applied to the carrier input jack near the center of the panel. When the input signal applied to the correlator is a suppressed carrier envelope, the switch is placed in the IN position in order to accomplish the demodulation of the input signal.

3.4.14 - Measure Switch

This switch has three positions; center off, momentary position marked SGL and a latching position marked RPT. These markings represent single and repetitive measurement respectively. This switch is only used in the R - θ position of the mode switch and is used to address a measure command for the R and θ measurement of a signal at the correlator input.

3.4.15 - Mode Switch

This is a three position rotary switch and must be positioned in the R - θ position to make phase and amplitude measurements.

In the Calibrate position, this switch isolates the correlator high input terminal, internally connects the generator output to the input amplifier and actuates a command signal in parallel to the repeat measure position of the measure switch. This enables a phase and amplitude measurement of the generator output signal without removing an input that may be present at the correlator high input terminal. In this position, however, it is necessary that the shorting link between the signal ground and LO correlator input terminals be connected, otherwise any signal present at the LO input terminal would affect the measurement.

DVM Position; this instrument has a self contained DVM circuit which is used for computation of the "R" vector in the analysis of a phase and amplitude measurement. It should be remembered that the instrument's primary function is not that of a DVM, so some of the normal features of a DVM are not available. In order to use the DVM the instrument must be in a measure complete status as indicated on the readout portion of the instrument. The ranges of the input range switch apply to the DVM; however, if the auto ranging option (AR) is included, it does not apply to DVM mode.

3.4.16 - DC Reject Switch and Level Control

This feature is used to null out a DC component which may be present in the input signal that exceeds the normal DC rejection of the instrument. Normal DC rejection without the use of this feature is limited to an amount equal to the full scale of the range selected. For example, in the 15 volt range,up to 15 volts of DC will be rejected automatically. In the 150 mv

range, 150 mv DC is rejected. This feature enables the rejection of up to 100 volts DC content of the input signal on any range. The following method is used: With the instrument in DVM mode, the stop switch in the "0" position, and the range switch in the 150 volt range, apply the input at the input terminals of the correlator. This will give an indication of the polarity of the DC offset. Position the DC offset switch to the appropriate polarity and adjust the level control until 0 reading is obtained on the DVM display. Advance to progressively lower input ranges and re-zero using the level adjust dial. After zeroing in the lowest input range, measurement of the signal can be accomplished without being affected by the DC component.

3.4.17 - Input Range Switch

The input range switch is a five position rotary switch on which there are four selectable ranges of peak voltage; 150 mv full scale, 1.5 v full scale, 15 volts full scale and 150 volts full scale The fifth position is for the optional Auto Ranging feature.

3.4.18 - Correlator Input Terminals

The correlator input terminals are located on the left side of the instrument and consist of signal ground, which is common to the signal ground on the generator side, the low side of the balanced input, and the high side of the balanced input. The instrument is provided with a shorting link between the signal ground and low terminal for single ended operation that is removable for balanced operation. The low terminal should NOT be left open while operating single-ended as it would be susceptible to noise pick up.

3.4.19 - Input Zero Adjust

This zero adjust is never necessary for making phase and amplitude measurements since any small offset in the input amp would automatically be rejected the same as a DC component in the input signal. However, it is desirable to zero the input amplifier to keep the offset from affecting a DC measurement made in the DVM mode.

3.4.20 - Power Switch

The power switch is an alternate action push button switch with an illuminated actuator to indicate the ON condition.

3.5 - Readout Display

The display section of the instrument consists of three general areas. The four numerical readout tubes on the left, display "R" during R - θ measurements and amplitude during DVM measurements. The four tubes in the right area display "θ". The area in the middle has illuminated wording which displays other pertinent information

3.5.1 - R volts Peak/DVM Display

This display consists of four digits capable of indicating from 0000 to 1900 with decimal point position according to range setting of the input. The number 1500 indicates a full scale reading which gives a resolution of one part in 1500 full scale. Logic circuitry limits an overload input to the 1900 count.

An input overload is indicated by a combination of this display and the Input Overload Light, depending upon whether the overload is due to the fundamental signal and/or DC and noise content of the signal. Since the input dynamic range is 200%, if the overload was due only to a fundamental signal within the 200% dynamic range, the overload would be indicated by a number greater than 1500 in this window.

3.5.2 - Instrument Status Display

This display consists of six indicators, as follows:

3.5.2.1 - The word Negative in the upper left portion of the center area is illuminated when the instrument is in the DVM mode and the voltage appearing at the correlator input terminals is of the negative polarity. The absence of this illumination indicates a positive voltage at the terminals.

3.5.2.2 - The word Measure located at the left center portion of the center area is illuminated while the instrument is in a measurement cycle for phase and amplitude. This display is especially useful in the case of very low frequencies, since several minutes are required to arrive at the final result and this indicator would serve to remind the operator that a measurement is in progress.

3.5.2.3 - The words Measure Complete located in the lower left portion of the center area are illuminated upon the completion of a phase and amplitude measurement. This indicator must be illuminated indicating the completion of a phase and amplitude measurement before using the instrument as a DVM.

3.5.2.4 - The word Lead, located in the upper right portion of the center area, is illuminated when the phase angle being displayed is leading the reference signal. The absence of this illumination indicates a lag angle.

3.5.2.5 - The words Power Overload, located in the center of the right portion of the center area, are illuminated when an internal power supply overload is present. A circuit senses the amplitudes of the internal supply and is triggered by any one of these various supply voltages going low due to overloading such as that which might occur during maintenance if a circuit board were plugged into a wrong socket. Over voltage protection is provided by use of a crow bar circuit in the power supply.

3.5.2.6 - The words Input Overload, located at the lower right portion of the center area, are illuminated when the sum of the signal and the offset appearing at the correlator input terminals exceeds 200% of the selected input range.

3.5.3 - θ Degrees

This display consists of four digits with a fixed decimal point. The phase angle indication is from 000.0° to 179.9°. This combined with the lead-lag information represents a total of 360° of phase indication.

3.6 - Option F Remote Programming (All Functions Located on Rear Panel)

3.6.1 - The functions available for remote programming are listed in Fig 2, Section 2, under J106. A switch is provided to enable the instrument to be compatible with positive or complimentary logic.

Logic Level Requirements:

Switch in "POS" position

Logical "1" = 4V ±1 VDC

Logical "0" = 0V ±0.5 VDC

Switch in "COMPL" position

Logical "1" = 0V ±0.5 VDC

Logical "0" = 4V ±1 VDC

3.6.2 - Before any information is programmed, it is necessary to put the Auto-Manual switch (on rear panel) in the auto position. This disables all front panel commands that are remotely programmable and enables the remote command buffers to take control; then the information can be applied to the data lines and the strobe command lines grounded to strobe the information in. To store the data in the input buffers, remove the strobe command before allowing any change in the data lines. Remote programming data applied to J106 will not interfere with manual operation if the strobe commands are in their high state.

3.7 - Option F- Remote Readout

3.7.1 - The functions available for remote readout are listed in Figure 1, Sec. 2 under J105. A switch is provided to enable the instrument to readout positive or complimentary logic.

Logic Levels Available:

Switch in "POS" position

Logical "1" = 4V ±1 VDC

Logical "0" = 0V ±0.5 DC

Switch in "COMPL" position

Logical "1" = 0V ±0.5 VDC

Logical "0" = 4V ±1 VDC

3.7.2 - The output is continuously available for remote readout from the time the output read command (Measure Complete) is given until reset by the following read command.

3.7.3 - The read command (Measure Complete) is a D.C. voltage that changes from 0 ±0.5V to +4 ±1.0V until reset by a measure command.

3.7.4 - The complimentary read command ($\overline{\text{MEASURE COMPLETE}}$) is a DC voltage that changes from + 4±1.0V to 0±0.5V until reset by a measure command.

3.7.5 - The read command (Measure complete and in range) is for use with remote readout when operating in auto-range. This command should be used when it is desirable to print ONLY in range readings, the command is a DC voltage that changes from 0±0.5V to +4±1.0V until reset by a measure command.

3.7.6 - The read command ($\overline{\text{MEASURE COMPLETE AND IN RANGE}}$) is for use with remote readout when operating in Auto-range. This command should be used when it is desirable to print ONLY in range readings. The command is a DC voltage that changes from +4±1.0V to 0±0.5V until reset by a measure command.

3.8 - Option AR (Also part of Option F) Auto Ranging

3.8.1 - The purpose of the option is to automatically change the range of the input amplifiers when the input is above or below certain levels. This is accomplished by letting the instrument cycle through an operation, testing the amplitude reading and allowing the instrument to cycle again if the reading is above 1600 or below 0100. Before re-cycling occurs, the range is shifted up if the reading is above 1600 and shifted down if the reading is below 0100. If the reading is between 0100 and 1600 no change occurs and the unit stops when the Measure Complete State is reached. If a voltage is applied to the correlator that is out of the range of the instrument, below .0100 or above 160.0 volts, it will continue to recycle without giving a measure complete signal.

Because it is undesirable to operate the bias control and Auto-Ranging simultaneously, the instrument automatically disconnects the bias control when an auto-range command is initiated.

The DVM Function is to be used for setting up the Function Generator to make frequency response measurements. To make these settings an auto-ranging feature is not necessary and is not incorporated in this instrument.

4 - THEORY OF OPERATION

4.1 - General Description

The 1410 Frequency Response Analyzer provides a repetitive electrical signal to an external system and receives an electrical return signal from the system under test. The instrument extracts two components of the return signal that are due to the input signal, one in-phase with the input called X, and the other 90° out-of-phase called Y. The two components are further processed to transform X and Y into an amplitude and electrical phase angle.

By using Fourier Integral Techniques, the component of the return signal in-phase with the output of the function generator is found by multiplying the return signal by a sinusoidal wave in-phase with the output signal. This product is integrated for an integral number of cycles. By the end of the integration time a D.C. voltage is created equal to the X component. In a like manner the input is multiplied by a sinusoidal wave displaced 90 electrical degrees from the function generator output. This product is integrated and the D.C. Signal created at the end of integration time is equal to the Y, or out-of-phase component of return signal. These integration times are equal but vary in time as a function of generator frequency. This is explained in a later section. The X and Y signals are further processed to obtain digital amplitude and phase readings which are stored in registers and displayed on readout tubes. The amplitude reading observed on the front panel is peak amplitude of the fundamental in volts. Phase is in electrical degrees, lead or lag.

4.1.1 - General Description of Overall Block Diagram

Drawing No. 881-5-01-602

To understand the instrument's function, it is necessary to study the overall block diagram and then refer to the sub-block diagrams and then to individual board schematics.

Referring to the overall block diagram (881-5-01-602), start with Block No.1. This is the master oscillator. The frequency of this unit is controlled by parallel BCD lines. There are four sets of four lines; three for three digits and the fourth for decimal point. The output of the oscillator unit is a pulse train whose repetition rate can be varied from .36 per second to 3.6 million pulses per second.

This pulse train is routed to the function generator via line No. 1 and to the system control block No. 10, where the pulse train is diverted to the X multiplier, Block No. 5 and the Y multiplier, Block No. 13, when required in the system cycle. Each pulse advances the system operation by one electrical degree, so dividing by 360 it

is seen that the system functions from .001 Hz to 10,000 Hz.

The Function Generator (Block No. 2) is stimulated by the pulse train on Line No. 1 and is capable of producing a sine wave, square wave or suppressed carrier signal with sine or square wave modulation. The output amplitude can be programmed (F Option) or set by front panel controls. The output is applied to line No. 2 to the system under test (Block No. 3).

The return signal on Line No. 3 is fed to the input amplifier (Block No. 8). The signal is amplified and applied to Line No. 11. A peak of 2.4 volts at this point corresponds to full scale. The input signal must now be routed and applied to the input of Block No. 9,the Multiplier Routing Card MR1. Three switching conditions are dictated by the control signals on control Route No. 4. These are:

Condition No. 1

Input signal, Line 11, connected to X multiplier, Line No. 6; and Y Multiplier, Line No. 12.

Condition No. 2

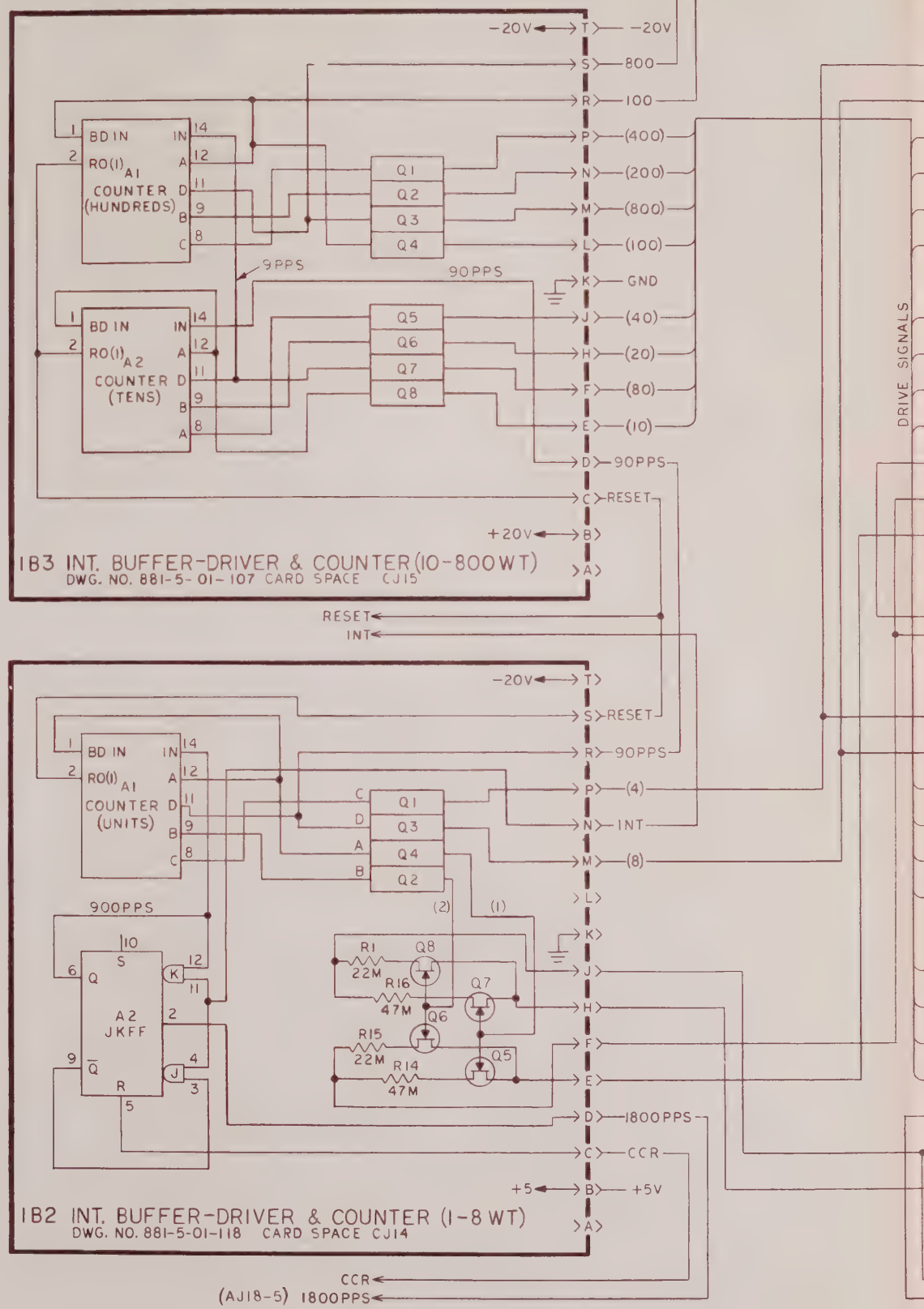
X signal, Line No. 5 connected to X multiplier, Line No. 6; and Y signal, Line No. 13, connected to Y multiplier, Line No. 12.

Condition No. 3

X signal, Line No. 5 connected to Y multiplier, Line No. 12 and Y signal, Line No. 13, connected to X multiplier, Line No. 6.

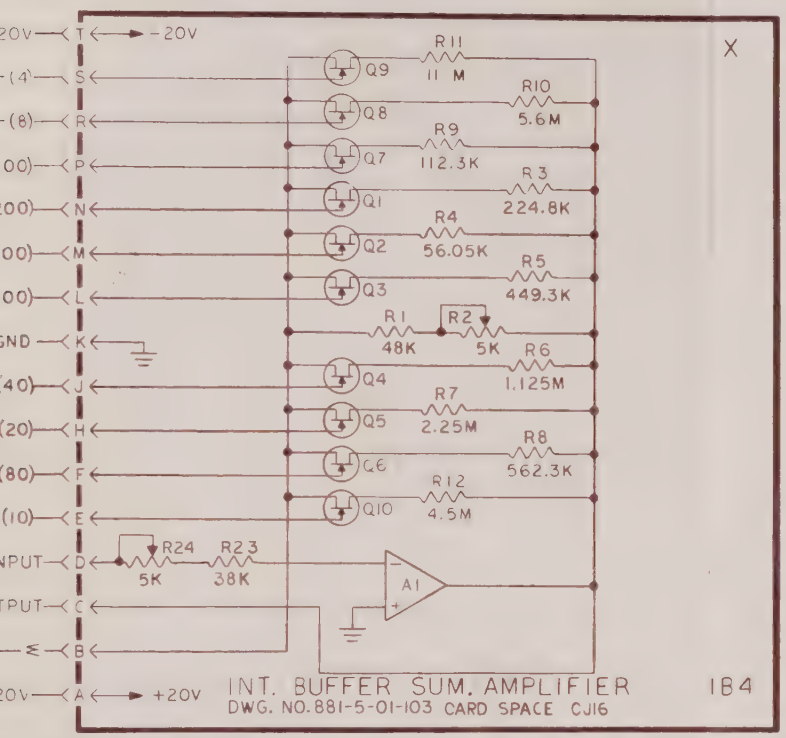
The return signal on Line No. 6 during Condition No. 1, will be multiplied by a sinusoidal function that is in phase with the output signal and will appear on output Line No. 7. The D.C. content of this waveform will be approximately 1.2 volts for full output. In a similar manner the same return signal on Line No. 12 will be multiplied by a sinusoidal function that is 90° out of phase with the output signal and will appear on output Line No. 14.

At the start of any half cycle of the output signal, the integrators will be turned on and will integrate the signals on Lines No. 7 and No. 14 for a period of one second plus the time necessary to complete a cycle so that an integer number of cycles are integrated. The integrators have automatic gain circuits that adjust for varying integration time. At the end of integration time a D.C. voltage is stored on the output (CJ16-C) of the X integrator which represents the magnitude of the return in-phase component and a D.C. voltage is stored on the output

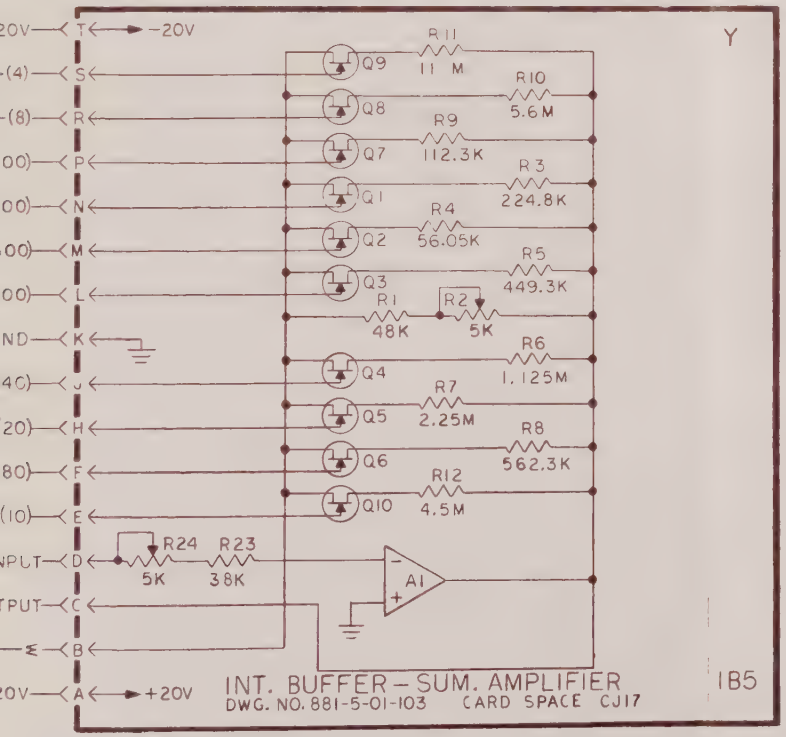

-20V
-20V
800
100
(400)
(200)
(800)
(100)
GND
(40)
(20)
(80)
(10)
90PPS
RESET
+20V
BD IN
RO(1) A1
COUNTER (HUNDREDS)
BD IN
RO(1) A2
COUNTER (TENS)
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
9PPS
90PPS
1B3 INT. BUFFER-DRIVER & COUNTER (10-800 WT)
DWG. NO. 881-5-01-107 CARD SPACE CJ15
RESET
INT
-20V
RESET
90PPS
(4)
INT
(8)
BD IN
RO(1) A1
COUNTER (UNITS)
900PPS
A2 JKFF
R1 22M
R16 47M
R15 22M
R14 47M
(2)
(1)
1800PPS
CCR
+5
+5V
1B2 INT. BUFFER-DRIVER & COUNTER (1-8 WT)
DWG. NO. 881-5-01-118 CARD SPACE CJ14
CCR
(AJ18-5) 1800PPS
DRIVE SIGNALS

NO.	REVISION	BY	CHK.	APP.	DATE

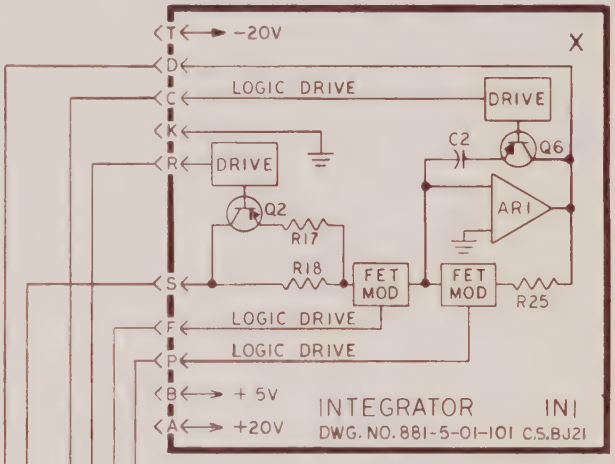
800 / 100 LOGIC TO CC-4 −M −L

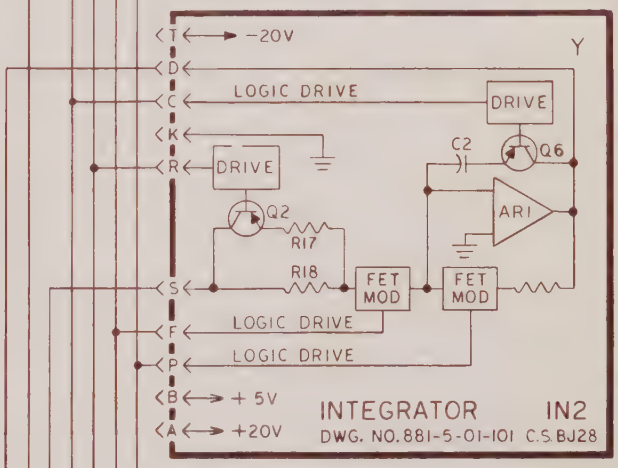


CJ16-C → TO MULT ROUTING (X)



CJ17-C → TO MULT ROUTING (Y)





SHORT INT. (0=ON) → TO CC5 (AJ19-A)
INT (0=ON) → TO CC5 (AJ19-H)
IO X INT → TO CC5 (AJ19-S)
SAMPLE (0=ON) → TO CC3 (AJ17-S)
X INT INPUT → TO X MULT (BJ19-S)
Y INT INPUT → TO Y MULT (BJ26-S)

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			DR. E. BACHMAYER	THREE DEC. PLCS. ±.005 TWO DEC. PLCS. ±.010 FRACTIONS ±1/64 ANGLES ±0°-30'		D	881-5-01-606	0			
			CHK.			DWG. SIZE	SCALE ~	SHEET 1 OF 1	DWG. REV.		
			APP.								
			APP.								
NEXT ASSY.	USED ON		MATL.	FINISH							
	1410										
APPLICATION											
12	13	14	15	16	17	18	19	20	21		

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(CJ17-C) of the Y integrator which represents the magnitude of the return out-of-phase component. The integrator outputs may be represented by the fundamental Fourier Coefficients or:

(1) X = X Integrator Output = $R \cos \theta$

(2) Y = Y Integrator Output = $R \sin \theta$

To resolve the Fourier coefficients into R and θ, the machine now must go into a compute cycle. The compute cycle is first discussed using trigonometric theory and then by logic theory. The Fourier analysis theory is covered from a more general view point in appendix A.

Trigonometric Theory

The angle θ is solved first by multiplying the integrator outputs by sin Z and cos Z respectively. Z is started at 0° and allowed to run until:

(3) $X \text{ xin } Z - Y \cos Z = 0$

Substituting (1) and (2) into (3),

(4) $R \cos \theta \sin Z = R \sin \theta \cos Z$

In order for (4) to be true, then,

(5) $Z = \theta$

And since Z is known, θ has been determined and is presented on the θ readouts.

At this point the two multipliers contain sin θ and cos θ respectively in their multiplicand registers and their inputs remain:

sin multiplier input = X integrator output

cos multiplier input = Y integrator output

Now the two input signals are reversed:

sin multiplier input = Y integrator output

cos multiplier input = X integrator output

Thus the two multiplier outputs become:

sin multiplier output = $R \sin^2 \theta$

cos multiplier output $= R \cos^2 \theta$

These two multiplier outputs are added to yield:

(6) $R (\sin^2 \theta + \cos^2 \theta) = R$

R is now converted to digital form with the internal DVM for presentation on the R readouts.

Logic Theory

To show how the instrument solves these equations, the operation will be discussed state by state. The state signals are created on the State Counter and Command Generator Board (CC6) and as each output line goes high a new set of operating conditions is initiated. During state one the polarity of the X component is determined. Pin D of CC6 (132) goes high activating the gate for the X polarity Flip Flop on Board CC7 (128). The state one signal is also applied to command input (J) of Board DVM 2 (126) which closes the switch from input (H) to the comparator A1. If the signal X at the input (H) is positive the output detect signal at output (C) goes high which makes input (R) of CC7 go high which activates the other input for the X flip-flop gate and output (J) of the Flip-Flop goes high storing the information that X was positive.

The clocking pulses for the state counter Board (132) are accurately timed at 3600 pulses/second. They are derived from the Primary Frequency Generator FR 1 (124). $\emptyset_1$ clock pulses at output (H) are used as standard timing pulses, and the $\emptyset_2$ pulses at output (M) are used when a half cycle delay is needed.

The state counter is now clocked to state two, a command signal appears at input (N) of DVM 2 (126) and the Y signal at input (M) is fed to the detector. If it is positive, a detect signal appears at output (C). The input for the comparator is turned on for state times two and three. This allows one clock period for circuit transients to diminish. During state three, the input (L) of CC7 (128) is energized gating the Y Pol Flip-Flop. If a detect signal appears at (R), output (F) will go high indicating the Y signal is of positive polarity.

After state three, output (S) of the state generator goes high for periods 4, 5, 6, 7, and activates command input line (E) of the Error Detect Board (126). The signal input (D) that this activates is the sum of the outputs of the X and Y multipliers created by amplifier A2 of DVM 1 Board (123).

The output (M) of Board (123) is now manipulated to obtain the value of the phase angle θ. This is initiated during state 5 (MEAS θ). Consider first a problem where the phase angle lies in the first quadrant, i.e., X positive and Y positive. The analog equation we present to the error detector is:

$$X \sin \theta - Y \cos \theta = 0$$

The sine table stored in the X multiplier will be stepped up from 0 in .1° steps and the cosine table stored in the Y multiplier will be stepped down from 90° until the left hand side of the equation passes from negative through zero. As it passes through zero, a detect signal is created. Refer to the Read Out Board Block Diagram No. 881-5-01-609. Input (N) of CC7 is turned on during state 5 allowing clock pulses to appear at output (S). These pulses are fed to the Phase Readout board where they clock the θ register through its various states until the equation is balanced. When the detect signal occurs, it appears at input (R) and inhibits the pulses at output (S). The phase angle is now stored in the readout tubes and a pulse is fed to the state counter to advance it to state six. A positive Y condition during state three will activate line (A) of CC7 (128) and the front panel lead light will be energized. If the phase lies in the fourth quadrant, output (F) of the Y polarity FF, CC7 (128) will be low indicating a negative Y. The θ equation cannot be balanced since both left hand terms are positive. This condition is sensed and the Y multiplier output is reversed by reversing the drive to Synchronous Demodulator Board MR3 associated with the Y multiplier.

If X is negative indicating 3rd or 4th quadrant location of the phase angle, the equation again cannot be solved. If X is made positive by reversing the drive to the Synchronous Demodulator Board MR2 associated with the X multiplier and X and Y are transposed, the equation, when solved, will have the desired θ less 90 electrical degrees. To overcome this a set signal for A3 on the phase readout board is generated whenever the X pol FF shows that a negative X exists. This allows the θ count to start at 90° to correct for axis rotation.

When the state five detect occurs, the state generator goes to state six and one clock pulse period later goes to state seven. During state six and seven the Multiplier input switch of the error detect circuit (126) remains activated. During state seven the following identity applies:

$$-(X \cos \theta + Y \sin \theta) + R = 0$$

During state seven, input (C) of CC7 (128) is activated allowing clock pulses to occur on output line (E). Activation is a signal going from +5V to zero. This clocks the R register on the Amplitude

Readout Board. At the start of state seven a precision negative - going ramp is generated by DVM-Board (123) at output (D). This is fed into terminal (S) of the Error Detector (DVM 2) and when it reaches a value equal to (X cos θ+ Y sin θ) a detect occurs, and the pulses out of (E) Board CC7 (128) cease and the R reading stored in the register and displayed on the readout light is equal to the amplitude of the fundamental of the return signal. The detect signal allows the State Counter Generator to go to state eight (MEAS COMPL) where the instrument remains at rest until called upon to perform another measurement.

To be able to study the operation in detail further block diagrams of sub-systems are available. Block No. 1, the master oscillator will be discussed next.

4.2 - Description of Master Oscillator

Block No. 1 Dwg. No. 881-5-01-607

Refer first to the upper left hand diagram, Primary Frequency Generator (124). This block is not related to the Master Oscillator but generates accurate timing pulses for the complete system. The circuit A1 is an accurate tuning fork oscillator that produces 3600 Hz. The signal is squared and differentiated and produces pulses at outputs (H) and (M) whose width is less than 15% of the period. The $\emptyset_1$ pulses are used as the basic timing and the $\emptyset_2$ pulses which are shifted a half period are used where a delay is needed. The pulses are +5 v high with 0 volts as reference.

Refer next to the Divided Clock Pulse board (120). A pulse train input occurs at (S) and is divided down by 1, 10, 100, 1000, 10,000 and is presented to the rest of the system on output line (R). This circuit performs the range changing dictated by the range deck of the front panel frequency selector switch.

When the range switch is in the 10^{-0} position, a zero will exist at input (P) Board (120). This places a high at A7-6, A7-8, A8-3, and A8-6 which sets decade counters A3, A4, A5, A6 in the nine state. When each decade counter is in state nine, the input at A8-13 will be high as the outputs of the decade counter are wired-OR at A2-6, A2-8, A1-6, A1-8. Four two stage NAND circuits are used on each decade counter to "NAND", a "one" with an "eight" output and invert.

With the 10^{-0} line activated all decades are in state nine, gate A8-12, 13, 11, is active and the pulses coming into input (S) go to output line (R) through two inversions on a one to one frequency basis.

When the range switch is in the 10^{-1} position, inputs (L), (M), (P) are high and input (N) is low. Counters A4, A5, and A6 are in state nine and A3 is free to count by 10. Every time A3 reaches state nine, A1-8 unclamps and the signal at A8-13 goes high. The next, or tenth, pulse passes to the output line (R) through two inversions provided by A8-11, 12, 13 and A8-8, 9, 10. The trailing edge of the pulse changes A3 to the state zero.

In a similar manner when 10^{-2} is grounded, A3 and A4 are allowed to count while A5 and A6 are locked in state nine. The output of A3 drives A4, therefore, and a count of 100 is produced. When 10^{-3} is grounded, A3, A4 and A5 are active for a count of 1,000. When no inputs are grounded a count of 9,999 between outputs must be reached so that A2-6, A2-8, A1-6 and A1-8 unclamp allowing A8-13 to go high so that the 10,000th pulse may pass to the output. This last procedure is for the 10^{-4} switch position.

The frequency range without this card would be 10 to 9,990 Hz and with the card at the lowest setting this can be reduced to .001 to .999 Hz. Additional ranges could be added with other stages, added externally, and connected to inputs (C) and (D).

Refer to the Pulse Counting Circuit (102). The pulse input rate at (T) ranges from 3600 Hz to 3.6 Mhz which corresponds to a frequency of 10 Hz to 10,000 Hz. This frequency is counted down to a controlled 3600 Hz which appears at output (C). A control action allows this value to be maintained.

If a front panel frequency is selected such as 0020, the count out will be set for 2 and the variable frequency pulse output will be controlled at 7200 pps which is equivalent to 20 Hz. Let us take the example (8620 X.1) on the block diagram. The pulse rate will be the integer 862 X 3600 pps. The following inputs will be high: 2F, 40F, 20F, 800F. When all the top AND lines are high a reset signal is generated to reset all the counters. A delay is incorporated so that all counters will have a reset pulse of sufficient width to reset all FF circuits. To get a reset signal, one side of all twelve top NAND circuits must have a zero. In the first decade, 1F, 4F, 8F, will be zero by switching and 2F is high. State two must exist in A1 decade for the four "unit" lines to be high. Lines 10F and 80F will be low, therefore A5 must be in state six for the "tens" lines to be high, likewise A9 must be in state eight for the "100's" lines to be high allowing a reset pulse to occur. The pulse output rate, therefore, will be 1/862 of the input rate, and the output frequency of the generator will be 8620 times the multiplier setting.

Refer to Master Oscillator Control Board (135). This board accepts the pulse output (C) of Board (102) and provides a D.C. control voltage for the Variable Frequency Pulse Generator that varies from +8 volts to -8 volts. The controller has integral action, and if the frequency is correct the output remains unchanged. If the frequency is too low the output will change in a positive direction at a rate proportional to frequency error. Likewise if the frequency is too high the

output will change in a negative direction at a rate proportional to frequency error. The resistors R7 and R9 set the + and - inputs of A1 at -4.5 volts. When a pulse occurs at input (R), the Flip Flop consisting of A4-1, 2, 3, and A4-8, 9, 10 is set in the state that A4-8 is high and A4-6 is then low which allows Q1 to turn on. Current will flow from ground through Q1 and R6 to the negative input of A1. Transistor Q1 will be turned on for a fixed stable time for each period. During this time the charge that flowed into the amplifier input must be equalled by a charge flowing from the amplifier input through R6 and R4 to a precision voltage source for the remainder of the period. If this condition does not exist, the output of A1 must drift up or down until a balance is achieved. A very stable frequency detector is created in this manner that will monitor when the frequency deviates from 3600 Hz.

The timing circuit consists of ramp generator A2 and comparator A3. The capacitor C4 is unshorted by switch S1 when a frequency pulse is received. When the output of A2 reaches 3.5 volts a detect is made and the FF is reset. This turns off Q1 a fixed time after each incoming pulse and reapplies a short to C4. The system now waits for another incoming pulse.

Refer to Variable Frequency Pulse Generator (137). The control voltage appears at input (S) where it drives Q1 of a differential amplifier Q1-Q2. If the control signal became more negative indicating the frequency was too high, the base of Q3 would become more positive reducing the value of the current from the current source created by Q3 and a large emitter degeneration resistor R8. This reduction of current flowing into C4 and C5 reduces the frequency of the saw tooth wave form created at the base of Q6. The saw tooth wave form at Q6 base is turned into a saw tooth current waveform in the collector circuit of Q6. This is fed to tunnel diode CR1 and when the current reaches the peak value of the tunnel diode the voltage across the diode suddenly rises applying a drive voltage to Q4 which in turn turns on Q5 which diverts the current from C5 and C4. When the voltage on Q6 base falls to a value that allows the collector current to fall below the valley current of CR1, the diode voltage suddenly drops, Q4 and Q5 turn off, and the rising portion of the sawtooth waveform is again initiated.

The flyback voltage appearing at the top of R11 is applied through two inverters to create a positive-going output pulse at terminal (M). The frequency of the sawtooth can be changed by changing the charging current and capacity to ground. The range of variation of the current source has a maximum value of 3 to 1. For frequency dial settings above 4,000 (range settings not a factor) the active capacitors will be C4 and C5 for the highest range. If the setting goes below 4000, line (N) and (P) will be low and line (R) will rise. This allows Q8 to turn on adding C6 to the circuit. The rest of Section 4.2 neglects the fixed zero of the frequency setting.

Refer to Capacitor Switching Board (136). For lower ranges this adjacent board with additional switches and capacitors is provided. Line (C) of the Variable

Frequency Pulse Generator connects to this board. If the frequency selector switch is set below 100, input line (S) and (R) are low and A5-10 is high. Since A5-9 is already high this makes Q5 conduct and C5 is added to the capacitor bank.

In a similar manner C4 is added below 040, C3 is added below 010, C2 is added below 004 and Q1 conducts for 000, shorting the capacitor bank. This obviously stops the action and produces zero frequency.

The master oscillator frequency can be controlled from a remote location using paralled BCD. The frequency lines desired are energized with +5V and those not desired are connected to +5V. See F Option specifications.

4.3 - Description of Function Generator

Block No. 2, Dwg. No. 881-5-01-608

The master oscillator clock pulses are fed to function generator boards FG 6 (117) FG 7 (117), FG 8 (114), and FG 9 (119). Consider first board FG 8 (114). The clock pulses enter (C) and go to the input of decade counter A1. This runs free continuously unless it is locked in state 9 by gate A7 if a low appears at (S), STOP 90°, or (R) STOP 0°. Every time A1 reaches state nine both inputs 12 and 13 of A5 are activated producing a low at A5-11. This in turn produces a high at either A3-3 or A3-11 depending on the signal on lines (H) or (E). Pulses appear at (F) when a $\overline{90°}$ signal occurs and at (D) when a 90° signal occurs. These are designated shift right (S/R) and shift left (S/L) respectively. The $\overline{90°}$ signal is a signal that is high between 0° and 90° and between 180° and 270°. The 90° signal is the inverse being high between 90° and 180° and between 270° and 360°.

Follow the S/R and S/L lines to inputs (F) and (M) of boards FG 6 (117) and FG 7 (117). If $\overline{90°}$ is active, S/R pulses occur at (F) every time the decade counter reaches state nine. Assume all Flip Flops A1, A2, A3, A4, on boards FG 6 and FG 7 are in the $\overline{Q}$ state. Inputs 3 of the J input of all FF's are high when state nine occurs. The J input of A1 FG 6 is activated because input 4 is high, and when state nine and the trailing edge of the clock pulse at input 2 occur, A1 will go to state Q. This activates input 4 of A2 and when state nine and the trailing edge of the clock pulse occur again A2 is triggered into the Q state. As each successive S/R pulse occurs another FF is turned on until all eight are in state Q. After ten degrees the signal (10°) at (D) goes high, after 20 degrees (20°) at (H) goes high, etc., until after 80 degrees (80°) at (R), FG 7 goes high.

Referring to FG 9 (119) when we reach 80° and the next S/R pulse occurs, the J input to the 90° FF is energized and the Q output goes high. The S/R pulses are now inhibited and pulses occur on the S/L line. The only input that can be activated is the K input of A4 on Board FG 7. When 99° is reached, this input is activated and A4

changes to state $\overline{Q}$ on the trailing edge of the clock pulse. When the next S/L pulse occurs, K of A3 is activated and A3 goes to state $\overline{Q}$. Each FF is successively turned off from right to left and returns to the original condition where all eight FF's are in the $\overline{Q}$ condition.

Referring again to FG 9, the trailing edge of Q of the 90° FF will toggle the 180° FF to a new state at the completion of each half cycle. The outputs of the 180° FF are gated to outputs (F) and (D) for driving FG 5 through the equivalent of a DPDT switch. When the phase switch is in the 0° position, input (C) is high, A3-1, 2, 3, is activated, A3-4, 5, 6, is activated and $\overline{Q}$ appears at (D) and Q appears at (F). When the phase switch is in the 180° position, (C) is low and the conditons are reversed with Q on (D) and $\overline{Q}$ on (F). With the circuitry described so far on boards FG 6, FG 7, FG8, and the FG 9 and with oscillator pulses being supplied to the decade counter A1, all the digital signals needed to generate a "digitally created sine wave can be observed on the output lines.

A sinusoidal wave with an amplitude of 5V is created at the output (S) of FG 1 by means of an operational summation amplifier. To create this output a sinusoidal current of amplitude .5 ma is injected at input (R). The current injection necessary to create ten degree steps as shown in Fig. 1 is derived from FG 2.

Figure No. 4-1

At the end of 10°, the signal on A1 of FG 2 goes low closing switch A1. The reference bus (L) is energized with a stable 5 volt source that changes polarity every 180°. This reference voltage is applied to the resistor bank R1-R8. Therefore, when A2 is closed an additional current 5/R2 is added. A3 closes at 30°, A4 at 40°, A5 at 50°, A6 at 60°, A7 at 70° and A8 at 80°. When 100° is reached A8 is opened, when 110° is reached A7 is opened, etc., and an approximation of a sine wave is created. At 180° the voltage is reversed and the opposite 180° of the sine wave is created.

The FG 5 board creates an output reference 5 v square wave by alternately turning on Q1 and Q2 and connecting the -6v reference voltage to the inverting and non-inverting input of the operational amplifier (A1). The 180° and $\overline{180°}$ logic signals occur on inputs (J) and (L) to provide stimulus for the transistor drive circuits.

To complete the sine wave approximation, the steps of the waveform are connected by 9 smaller, uniform steps. The additional current injection necessary would have a waveshape similar to Fig. 2.

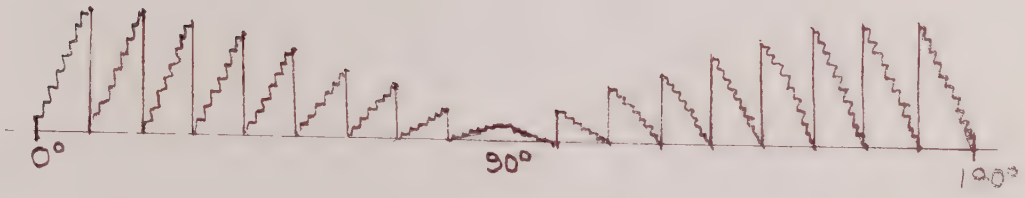


Figure No. 4-2

It would be a series of triangles that decrease to zero as 90° is approached and reverse direction as 90° is reached and increase in value to maximum at 180°. This waveform would repeat itself in the opposite polarity for 180° to 360°.

A stepped voltage that starts at .05 volts and increases .1 volt for each degree to .95 at 9° and drops to .05 at ten degrees, etc. appears at input (J) and (L) of FG 3. The output of FG 3 (H), (M) is summed into the amplifier on FG 1.

Between 0° and 10° all the switches A1-A8 on Board FG 3 are closed and the largest triangle of current is injected into the summing point. When 10° is reached, switch A1 opens and a smaller triangle is created. This continues progressively and when the operation is between 80° and 100° all switches are open and the weight consists only of R9. In a similar manner between 100° and 110° switch A8 closes and the weighting increases to a maximum at 170° to 180°.

The Board FG 4 is used to create the .95v triangular wave needed at input (J) and (L) of FG 3. The input to the operational amplifier is coded in binary in a 1, 2, 4, 8 weight manner. In the range 0° to 90° or 180° to 270°, switch A1 is energized at state 1°, A2 is energized at state 2°, A1 and A2 at state 3°, A3 at state 4°, etc., until A1 and A4 are energized at state 9°. During the periods 90° to 180° and 270° to 360° the action is reversed. When state 1° is reached A4 is energized for a 8 weight. When state 2° is reached A3, A2, A1 are energized for a 7 weight, etc. The switching logic required to drive inputs (S) (R) (P) (N) of FG-4 is developed on Board FG 8. When the unit is in the 90° state, the switching transforms directly, i.e., when state one exists, the 1° switch (J) line is low indicating an on condition for the 1° switch. When state two exists the 2° switch (P) is low.

When state three exists, lines (J) and (P) are low, etc. The outputs 1, 2, 4, 8, on A1 are coupled out through one inversion through A3-8, 9, 10; A5-4, 5, 6; A2-4, 5, 6; A5-8, 9, 10 respectively.

When 90° is reached a different set of conditions exist. For 2°, 4°, 6°, 8°, the 1 output of A1 goes through A4-11, 12, 13 and presents a zero at output (J). For 2°, 3°, 6°, 7°, the 2 output of A1 passes through A5-4, 5, 6 and presents a zero to output line (P). The line for the 4° SW goes to a low, which is an "on state", when we have (4 and $\overline{2}$) or (2 and $\overline{4}$) from the decade counter. This is accomplished by circuits A6-11, 12, 13; A2-8, 9, 10; A4-1, 2, 3; A4-8, 9, 10; and corresponds to state 4°, 5°, 2°, 3°. Similarly line (M) is activated when the counter is in state 1°. We then have the following activation table:

State 1°	8W	-	-	-
State 2°	-	4W	2W	1W
State 3°	-	4W	2W	-
State 4°	-	4W	-	1W
State 5°	-	4W	-	-
State 6°	-	-	2W	1W
State 7°	-	-	2W	-
State 8°	-	-	-	1W
State 9°	-	-	-	-

To this point the circuitry covered in the discussion will create a sine wave of 5V amplitude at output (S) of FG-1 which can vary from .001 Hz to 10,000 Hz. This signal is fed to the front panel gain adjust pot. The wiper goes to relay contacts K1 on board 0A1 and then to input (R) of 0A2. Amplifier 0A2 builds the signal up to 15V peak which is the maximum output driving signal.

If the front panel 1.5V - 15V switch is in the 1.5V range, relay K1 of 0A2 is energized and the 0A2 gain is reduced by ten.

An automatic programming option board 0A1 can be provided as shown which replaces input resistor R2, Board 0A2 with the resistor bank R1-R9 of 0A1. As various command lines are grounded, corresponding output peak voltages can be commanded. If, for example, the peak of the output sine wave was to be set at 12.1 volts, lines (B), (L), and (T) would be grounded.

The 0A2 output can be biased from +10V to -10V by using input resistor R1 and the front panel bias adjust potentiometer. If the AC-DC switch is placed in AC position, the relay of FG 5 is connected to the Carrier Amplifier output (C) of board FG-1. This allows the Function Generator to modulate a carrier introduced at the front panel jack and produce an output signal with double side bands and suppressed carrier.

4.4 - Description of Input Amplifier Circuitry

Block No. 8, Dwg. No. 881-5-01-611

The input Amplifier, Block No. 8, consists of 4 boards, IA1, IA2, IA3, and IA4 whose block diagram is shown in Drawing No. 881-5-01-611. The function of the subsystem is to adjust the signal to a level that the multipliers can process with accuracy. This output occurs on Line No. 11. This is line (M) of Board IA4 (148) and the voltage at this point will be 2.4 volts peak from a low impedance source.

The inputs occur at the HI input J5 or LO input J6. The HI input signal passes through input selector switch S2-C to Amplifier IA1 (H) in the R AND θ MODE, and DVM MODE. In the CAL MODE the output of the instrument is connected to the amplifier input. Amplifiers IA1 and IA3 are identical and each consists of an operational amplifier with input and feedback resistors and a relay means of switching these resistors. For range 1 (150 mv) input (F) is grounded and relay K1 is energized. This sets the system up with 100K input impedance and 400 K feedback and will create a full scale signal of .6V at output (D). For range 2 (1.5V) no relays are energized and the input resistance is 1 megohm and the feedback resistance is again 400 K. For this range 1.5 volts input is required for .6V output. For range 3 (15.0) input (C) must be grounded, energizing relay K3. This reduces the feedback resistance to 40K and 15 volts input is required for full scale. For range 4 (150 V) relay K2 is energized by grounding input (E). This reduces the feedback resistance to 4K and 150 V input is required for full scale.

The outputs of IA1 and IA3 are fed to inputs (S) and (R) of the Mixer Amplifier IA4. The mixer amplifier has a gain of four and inverts the signal on (R) and non-inverts the signal on (S). The difference signal between J5 and J6 is the only signal that will appear at output (M).

If the Demodulator Switch on the front panel is placed in the "IN position, relay K1 of Board IA4 (148) is energized and the Carrier Demod IA2 (141) is connected between the mixer and the multiplier routing board. The carrier Demod is basically a synchronous demodulator and unity gain amplifier. Transistors Q3 and Q4 are turned on alternately at the carrier frequency producing a rectified output at (R).

4.5 - Description of Multiplier Routing

Drawing No. 881-5-01-125

This block is a single board. Refer to schematic MR-1 (125). A "Compute" interval is created by combining the signals at (J), (H), and (F). This signal is high after integrate and before state 8 (measure complete). During the time that the compute signal is low, A2-8 will be high and transistor Q7 is turned on. This, in turn, turns on switching transistors Q1 and Q4. Referring to the main block diagram, during this time (all time other than computation time) the signal on Line No. 11 is fed to the X multiplier on Line No. 6, and to the Y multiplier on Line No. 12.

During the MEAS θ (State 5) interval when X is positive, the output of the X integrator buffer is connected to the X multiplier and the output of the Y integrator buffer is connected to the Y multiplier. This is Line No. 5 connected to Line No. 6 and Line No. 13 connected to Line No. 12. This is accomplished by a Meas θ signal on 2 and X + signal on 1 of A3. A3-3 goes low and A3-6 goes high which cause Q2 and Q6 to close to cause the above described switching condition.

If X is negative during Meas θ interval, input 4 and 5 of A2 go high, A2-6 goes low, A2-11 goes high and transistors Q3 and Q5 close reversing the connections and connecting Line 5 to Line 12 and Line 13 to Line No. 6. This rotates the phase by 90°. Refer to the general description for an explanation for this action.

When X is positive and the instrument is in state 7 (Meas R), X and Y are transposed as in the above paragraph. This is accomplished by a high at A2-2, and A2-1 which creates a low at A2-3, and this causes A2-11 to go high. This creates the term:

$$X \cos \theta + Y \sin \theta$$

needed to solve for R.

If X is negative and the instrument is in state 7 (Meas R), it is necessary to rotate the axis 90° and, therefore, it is necessary to transpose back to the conditions which

require that the X integrator output goes to X multiplier and the Y integrator output goes to the Y multiplier. This is accomplished by a high on A3-9 and A3-10 which makes A3-8 low which activates A3-6 turning on Q2 and Q6.

4.6 - Description of X Multiplier Circuit

Block No. 5, Dwg. No. 881-5-01-605

Refer to Block Diagram (605). The signal from the multiplier routing board MR-1 (125) appears on Line No. 6 and (P) of the Synchronous Demodulator Board MR-2 (116). During integration time the signals on (M) and (L) are the $\overline{180°}$ and 180° drive signals at the function generator frequency which are used in the Demodulator to synchronously rectify the incoming signals. During computation time this circuit is used as a polarity changer, and a set of several conditions can determine the inputs to (M) and (L). These logic conditions are shown on XYM 7 Board.

Boards XM 1, XM 2, XM 3, are identical to Boards in the Function Generator and the Summation Amplifier XM 4 performs the same function as the amplifier on FG 1 board.

The XM 4 board, has in addition, however, a frequency compensation circuit which provides a negative D.C. offset current to amplifier A1 which is directly proportional to frequency.

In addition to the above boards the .1° Generator Board XYM 1 (109) is needed. This allows the 1° Generator (121) to be stepped in 0.1° steps in the computation mode. One half of the board is for the X Multiplier and one half for the Y multiplier.

The output of the multiplier on Line No. 9 and Line No. 7 is the input on Line No. 6 multiplied by sin θ. Since the switching networks cannot create polarity, the input is switched every 180° to simulate the fact that Sin θ, for a complete cycle, contains both positive and negative values.

4.7 - Description of Y Multiplier Circuit

Block No. 13, Drawing No. 881-5-01-604

This circuit is essentially identical to Block No.5. The .1° Generator for the Y multiplier is located on XYM-1. It will be noticed that the logic drive signals are not the same. By a rearrangement of inputs this multiplier is shifted 90° in phase and becomes a cosine multiplier. The logic drive circuitry for the X and Y multipliers is shown in Block Diagram Drawing No. 881-6-01-612.

4.8 - Description of X & Y Integrators

Block No. 6 & No. 14, Dwg. No. 881-5-01-606

The X integrator consists of analog boards IB4 (103) and IN1 (101) and the Y integrator consists of analog boards IB5 (103) and IN2 (101). The two integrators share the logic circuitry on IB3 (107) and IB2 (118). The integrator inputs are (S) (101) and come from the X and Y multipliers. These are direct connections with no switching. The average input value for full scale output is 1.2 volts and provides an output voltage on (D) of 4 volts after 1 second of integration.

The integrator can work in several different modes and the switching for all possibilities will be discussed. Consider first "X10 integrate". This condition requires ten times the integration time, therefore, the signal to the integrator must be reduced by ten to compensate. This is accomplished by permitting input (R) of IN1 and IN2 to go high which opens Q2 and increases the input resistance by ten.

When the integration time is reached, input command (F) of IN1 and IN2 goes low and the input signal is fed to the integrator. Before integration the integrator is clamped with R25 and the FET MOD switch. At integrate time, (P) goes high and the clamp is removed. The clamps stay removed until state 8 is reached. At the end of integration, the input signal is disconnected from the integrator by a high appearing on (F). The value of X is stored at output (D) to be used during the computation period. For frequencies above .5 Hz, the integrator is in conventional mode, input (C) is low and Q6 is closed. When the frequency is below .5 Hz a different mode of operation is set up and switch Q6 is closed for a fraction of each 1° period. Integration will continue until one full cycle of the function generator is completed but capacitor C2 will be connected to the circuit for a total of one second. Whenever Q6 is open in this mode the amplifier will be clamped. The logic commands involved in the above modes will be discussed in a later section on control logic.

The output of the integrators drive the inputs of the variable gain buffers. The buffers are necessary because integration time must vary because integration must include an integral number of cycles. If an integration of 1 second were taken for 1,000 to 10,000 Hz a very small error would result, (1 part in 1,000 if integral cycles were ignored) but as .5 Hz is reached, integration time must be increased to 2 seconds as one second of integration would have no meaning. Integration for 2 seconds for .5 Hz would have twice the reading as 1000-10,000 Hz for two seconds, therefore, the gain has to be reduced by 1/2. This requires that the feedback conductance be increased in a linear manner with time starting from the one second point. One second is divided up into 900 parts and the following resistors are connected for the following counts:

COUNT	RESISTANCE
1	47 meg.
2	22 meg.
4	11 meg.
8	5.6 meg.
10	4.5 meg.
20	2.25 meg.
40	1.125 meg.
80	562.3K
100	449.3K
200	224.8K
400	112.3K
800	56.05K

On IB4 and IB5 transistors Q1-Q10 are the switches for these resistors. The switches for the 1 and 2 count are Q5, A6, Q7, A8 on Board IB2 (118). The drive voltage for these transistors is -15 volts off and 0 volts for on.

On board IB2 (118), a continuous 1800 Hz square wave occurs at input (D). This is derived from the precision 3600 Hz source. When inputs 4 and 11 of JKFF A2 are activated by an Integrate signal (high) on input (N) an output square wave of 900 Hz is created at A2-6. This drives counter A1 whose 90 PPS output is fed to IB3 (D) as shown. This signal drives A2 counter which in turn drives A1 counter.

The operation of the counter then is as follows: The counter is set to zero before integration time. When integration time occurs, the counter is unlocked and will count to 900 in one second. At this time an 800 and 100 output at (S) and (R) IB3 (107) is fed to CC 4 where the information is stored that one second has occurred and a reset signal is sent back to the counters. The counters immediately start counting again and when the end of integration occurs the count is stopped and held during computation. The count stored is equivalent to the time past one second that was required to make the integration. The 1, 2, 4, 8, outputs of the decade counters energize the drivers shown. These

drivers energize the necessary switches on IB4 and IB5 to compensate the gain for the time past one second that was necessary for integration. The circuitry for integrator switch driving, resetting of counters, and one second storage, will be discussed further in a later section.

4.9 - Description of Readout Block Diagram

Drawing No. 881-5-01-609

The top three blocks on the Readout Block Diagram are shown semi-pictorically, i.e., looking from the back of the instrument, the readout tube V1 would be to the left with A5 and A1 in back as shown with the other readout tubes progressively to the right. Each of the Readout tubes is driven by a decoder/driver Integrated Circuit Package. These in turn are driven by a Decade Counter except for the most significant position which is driven by a JK Flip Flop. The counters are set up in cascade and have the capacity to register a count up to 1999. The counters are clocked by 3600 Hz pulses occuring on input (2) for the θ register and input (46) for the R register.

The gating for these clock pulses is accomplished by circuits A5 and A3 in the lower half of CC7 (128). During Measure θ time interval, gate A5-4, 5, 6, is open and $\emptyset_2$ clock pulses appear at output (S). When a detect or over range signal appears at input (R), A5-11, 12, 13 shorts output (S) to ground. When state 7 (Measure R) is reached, gate A3-4, 5, 6 is opened and clock pulses occur on output (E). Again when detect occurs line (E) is shorted to ground by A5-1, 2, 3. The operation of the other circuitry for storage the polarity of X and Y is explained in Section 4.1.

A restraint is put on the θ reading which provides a readout limit at 89.9° if a detect signal hasn't been obtained when this state is reached. A restraint is also put on the R reading which provides a readout limit at 1900 if a detect signal hasn't been obtained when this state is reached.

The required logic to perform these functions is shown on CC9 (129). The detect signal appears at input (A) and A3-11 goes low. A low at either input 4 or 5 of A3-4, 5, 6, will create a high detect signal at output (C). If a detect signal does not occur and the machine is in the Measure θ state when 89.9° occurs, inputs 1, 2, 4, 5, 9, 10 will be high and output A1-6 will go low creating a detect signal at output (C). If 1900 is reached in the R register, lines (F), (H), (J) will go high and output A1-8 will go low creating a detect signal on output line (C). For resetting the registers either the command chain reset (CCR), which occurs at the beginning of each measurement, or the DVM reset is used. These come out on output line (M) of CC8 (140) as positive pulses. The positive pulse is used to reset the decade counters and an inverted pulse from A2 on output (P) of CC5 (143) is used to reset the JK Flip Flops, A4 and A4A, on the readout boards.

Referring to Drawing No. 881-5-01-115-2, the Indicator Light section of the Readout Board operates as follows: When a Meas. Comp. signal appears at input (38) A10-6 goes low and Q1 turns off. This allows the MEAS COMPL light to turn on. The Measure

light works in the same manner. The DVM Polarity light will become energized indicating a negative reading when both inputs (40) and (41) are high. A high on (40) indicates the instrument is in DVM mode and a high on (41) indicates a negative condition. The output of the mixer amplifier is sensed and if it exceeds plus or minus 5 volts, the INPUT OVLD light is activated. This will lock in on a transient and is reset for each reading. The LEAD light is activated directly by light driver Q1 located on Board CC7 (128). This light is energized when Y is positive indicating a leading phase angle. An unbalance of the voltages at inputs (95) and (80) which go to the alarm circuit on the 20 V regulator board (122) will energize the POWER OVLD indicating that one of the voltage busses (+5 V, -20 V, +20 V) has changed in value.

4.10 - Description of Power Supply

Drawing No. 881-5-01-603

The power supply consists of four D.C. sources, three of which are regulated. The sources, their output voltages and current capabilities are:

+5 V	3A	Regulated
+20 V	1.2A	Regulated
-20 V	1.2A	Regulated
+200 V	50 ma	Unregulated

As seen from the drawing, the 200 V supply uses a half-wave rectifier, a bridge rectifier circuit is used of the plus and minus 20 volt supplies and a full-wavecenter tapped rectifier circuit is used on the +5 Volt supply. Transistors Q1, Q2, and Q3 are the silicon pass transistors for the supplies.

A thermostat set at 120° C senses the heat sink temperature and will disconnect primary power under overload or high temperature conditions. Refer to ±20 volt regulator board schematic 881-5-01-122. For the ±20 V regulators, identical circuits are used. Resistors R6 and R16 are the adjustments for setting the output voltage. Resistors R3 and R13 are the adjustments for current limit. This is a foldback circuit and in short circuit condition, the current will fall back to about 30% of the overload set-point.

Elements CR1 and CR2 form a crow bar circuit which will fire the SCR if the voltage should rise to 22 V. This places a short through R9 across the rectifier input and blows the main line fuse. The + 5 V regulator and Diode Board Dwg. No. 881-5-01-147 contains rectifiers CR1-CR9 and the +5 V regulator. This regulator is the same as the ±20 V

regulators except that it is wired for constant current for overload conditions. When the load current reaches the value set by R4 the voltage starts to drop but the current no longer increases and is regulated at the overload setting. This supply is also protected for over-voltage by means of a crowbar circuit.

4.11 - Description of Control Logic (Partial)

CC-1, CC-2, CC-3, CC-4, CC-5

Block Diagram Dwg. No. 881-5-01-610

The five cards associated with Block Diagram 881-5-01-610 provide the control logic required to take the machine up to the end of integration, by which time the X and Y components of the return signal have been determined. This includes the control circuitry required to put the integrators into four different modes of operation. These modes are:

Mode No. 1 - Normal Integration for frequencies greater than .5 Hz

Mode No. 2 - Normal Integration for frequencies less than .5 Hz

Mode No. 3 - X10 Integration for frequencies greater than .5 Hz

Mode No. 4 - X10 Integration for frequencies less than .5 Hz

In the Mode No. 1 the integration starts at a zero crossing of the function generator and ends when an integral number of cycles has been completed after a one second period elapses (measured from the start of integration).

In Mode No. 2, the integration starts at a zero crossing of the function generator and ends precisely one cycle later. The integrator buffer is locked at 100% gain- the gain required for one second integration time. Since the time of a cycle can vary, the integrator is activated every electrical degree for a period of 1/360 of a second. In this sample and hold technique, the time is the equivalent of one second integration time for one cycle.

In Mode No. 3, the clock rate is reduced by a factor of ten. To compensate for the fact that the integration time is increased by ten, the input impedance is increased by a factor of ten. The output reading will be the same as for X1. The longer integration time will increase by an order of magnitude the rejection of a closely spaced non-synchronous "noise" signal.

In Mode No. 4, the integration time is increased by ten by allowing the operation for X1 Int., to cycle ten times. The output will be ten times normal integration, therefore, the input resistance must again be increased by a factor of ten.

To study the circuitry start with CC1 (144) and CC2 (131) and the associated timing diagram, Figure 4.3 following Section 4. The $\emptyset_1$ and $\emptyset_2$ clock pulses occur every 1/3600 of a second displaced by one-half period. The next waveform, CTM, is shown for SGL operation of the front panel MEASURE switch. Input (C) of CC1 is grounded, transmitting a momentary ground to (S) of the A3 (Command To Measure) FF. This sets output Q high. The CTM FF arms (J) of the MIP (Measure in Progress) FF. Input 4 is high because the .4 sec one-shot circuit is not activated. The next $\emptyset_2$ clock pulse toggles the MIP FF to the Q state. Between the time CTM FF goes high and MIP FF goes high a negative going CCR (Command Chain Reset) pulse is created at the output of A5-8. This is used to reset circuitry before the machine goes into "Measure in Progress".

Following the waveforms to the right, it is now assumed that the front panel switch is in the repeat mode. After the machine finishes operation; State 8 (Measure Complete) goes high and a .4 sec. inhibiting delay is activated. The delay holds the CTM FF in the reset mode. This delay is incorporated to allow State 8 to be long enough for the integrators to be reset. After the delay, the CTM is armed for a "J" operation. Since Input (H) is grounded, A2-8, 9, 10 makes 4 of CTM FF high. The next $\emptyset_2$ clock pulse will therefore put CTM FF in the Q state. This same pulse can put MIP FF in the $\overline{Q}$ state since the .4 sec delay no longer inhibits J and K. Since CTM FF goes high and MIP FF goes low, CCR goes low and resets the state generator. This resets state 8 to zero. The next pulse toggles MIP FF to the Q state and the CCR goes to a high state. The operation stays in this mode until state 8 again occurs and the action repeats.

The CCR signal resets circuitry, and the MIP signal starts the synchronizing procedure. Refer to CC 2 (131). When the MIP signal goes high, the A1 and A3 FF's are unclamped and remain in the $\overline{Q}$ state. When the Function Generator 90° signal goes low at input 2 of A1, the FF will go the Q state arming input J of A2. The A1 FF will go to state Q at 90° or -90° for "USE" mode, and 0° or 180° for "45° and 90°" setting of front panel control. When A1 goes high the downward edge of the Sync Pulse is created. The J operation of A2 can now be activated by a negative going signal at input 2 of A2. This can be created by A4 which is a three circuit "wired OR". Point 2 will drop as shown by the logic equation shown near Block Diagram (881-5-01-610), part CC2. As A2 goes high for these conditions, the Sync Pulse terminates in a high condition.

The sync pulse resets the Correlator shift register (XYM3, XYM4), and the 180° and 270° FF (XYM7). The 90° FF, however, is set to the Q state by the CCR. Referring to A7 and A8 on CC3 (133), the following logic equation is implemented:

$$\text{COR DCP} = (\text{STC})\ \overline{(1\ \text{SEC})} + \text{INT}$$

which states that the Divided Clock Pulses for the correlator circuitry will be gated on when STC goes high and will remain high until one second of integration time has elapsed. Refer to "Timing Diagram for CC1 (144) and CC2 (131)" for waveforms. After this time the integrate signal holds the gate open and the gate closes after integrate time. The gate opens on the 179°, 44°, or 89° count and the next pulse clocks the 90° FF from high to low, activating the INT FF on CC4 (139). The first pulse also activated the 1° counter, A1, on XYM 6 (130) which was in the 9° state. The above operations synchronize the Function Generator and Correlator at 0° and starts integration at this time.

Referring now to CC3 (133), this board determines before the integration period if the frequency is below .5 Hz and if so, activates a circuit that stores this information. If this conditon exists, a circuit is activated that creates a "SAMPLE" signal that is 1/360 second wide that occurs every electrical degree.

If the frequency is below .5 Hz, a signal, DTS, (Decision to Sample), is created. Refer to A4. The R (0) 1 and R (0) 2 inputs must both be high to set the counter to zero. The outputs A, B, C, D are the states 1, 2, 4, 8 respectively. During "Not Integrate" time, R (0) is high and the Generator Divided Clock Pulses, periodically reset the counter. If the counter A4 counts to 21 and the counter A5 counts to 2, which is the equivalent of 20 counts, before the Gen DCP can reset the counter, the time to reach 21 is greater than 2/360, therefore, we know that the Generator DCP pulses are occurring at a rate less than an equivalent .5Hz. The 21 count activates input (9) and (10) of A6 and output (8) goes low. A low on A6-5 activates the bi-stable circuit created by A6-4, 5, 6, and A6-11, 12, 13. This places a low on Line (L), DTS, which is a DTS command.

If the decision is "Not to Sample", input 1 and 2 of A6 will be high at integrate time and A6-3 will go low holding A1 in the set state. The "Sample" signal on output (S) will remain high during Integrate time and at end of integration the (R) input of A1 will go low resetting A1 and allowing output (S) to go low.

To understand what happens if the decision is "To Sample", refer to the timing diagram for CC3 (133), which is Figure 4.4. At the time of a gen. clock pulse, the INT signal will go high. At the same time the reset of A1 and the set of A3

are unclamped. The inputs 3 and 4 of A3 are high activating the J input. The following $\emptyset_1$ pulse puts A1 in the "Sample" state. The reset zero input (R (0) 1, R (0) 2) of A2 is unclamped and the counter counts to state 9 when the inputs 11 and 12 of A1 are activated. The 10th pulse after "Sample" is activated, therefore, toggles A1 FF back to $\overline{Q}$. The operation then repeats when the next Gen DCP occurs. Each sample pulse will, therefore, be 1/360 second long which makes the total integration time equal to one second.

A source of reference pulses at 360 pps are needed at output (H). These are obtained by using the output pulses from counter A4, and are needed for X10 Integration at frequencies greater than .5 Hz. When Integration occurs, input 2 of A4 goes low and the counter runs free.

Refer next to CC5 (143). Three signals are needed to control the integrator boards:

1 - The $\overline{INT}$ signal, when it goes low, activates the input switches.

2 - Output (J), when it goes low, closes the switch for the integrating capacitor. The equation is: Closed = $\overline{INT}$ + SAMPLE, which states that the capacitor switch will be closed at all times other than integrate time in addition to when the Sample signal is present. During normal integration (X1), the Sample signal will follow the Integrate signal.

3 - Output (C) when it goes low, closes the switch for shorting the Integrator amplifier. The logic equation would be Shorted Amp = (INT) ($\overline{SAMPLE}$) + MEAS COMPL + BEFORE INT. The first term states that during integration and between sample periods the integrator amplifier will be shorted. This is implemented by A7-11, 12, 13, and A8-8, 9, 10. The second term is activated by a high at input (A) which creates a low on A4-3, which creates a high on A4-8, which creates a low on A4-6. For the last term, the CCR sets the bi-stable circuit A4, 11, 12, 13 and A4-8, 9, 10 to a high on A4-8, which puts a low on A4-6. At integration time this circuit is reset and this term removed.

The rest of the circuitry on CC5 (143) is associated with terminating the integration time. If a high appears on line (L), this will place a high on input 11 of A3 of board CC4 (139). When this input plus the "1 second" input occurs, the INT FF can be clocked to a $\overline{Q}$ state by a falling edge of the cor. 90° signal which occurs at 0° or 180°. Output line (L) of CC5 is manipulated to prevent activating the INT FF at 180°. It is also held low for ten integration periods in Integration Mode No. 4.

Refer to the Timing Diagram for CC4 (143) which is Fig. 4.5. The A9 FF is reset by CC4 and is toggled by means of the $\overline{80°}$ correlator signal as shown. The gate A7-4, 5, 6 is closed when we have ($\overline{DTS}$) ($\overline{10 \text{ X } INT}$) which puts a low on A7-10 which makes A7-5 high.

The "Int Period Control" signal is as shown and inhibits the INT FF at the 180° point. At the 360° point, the INT FF can return to the $\overline{Q}$ state.

In the (DTS) (10 X INT) state, input 10 of A7 is high and the counter helps control the "Int. Period Control" signal. In this state the operation starts out as before until the trailing edge of A9-Q occurs. This clocks counter A1 to the one state and input 9 of A7 goes from low to high and A7-8 goes low clamping output Line (L) in a low state. The counter will count the pulses on A9-Q and when a count of ten is reached indicating ten periods have elapsed, input 9 of A7 goes low. A7-8 goes high activating the output line (L) and integration will terminate on the next negative going edge of correlator 90°.

Refer next to CC4 (139). The output line (S) provides reference pulses for driving the weighting circuits of the integrator buffers. These pulses are 1800 pps for X1 integrate and 180 pps for X10 integrate. Circuit A2 divides the rate by two and Circuit A1 does the switching for X1 and X10 integrate.

The action of the INT FF has already been discussed. Circuits A4 and A5 are used in conjunction with timing one second, storing one second information, and resetting IB2 and IB3 integrator buffer boards. There are two modes of operation for these circuits: DTS (Decision to Sample) and $\overline{DTS}$ (Not Decision to Sample).

Consider DTS first. Input 12 of A4 is low and inhibits A4 from returning to $\overline{Q}$ state. Input 4 of A5 is low and removes A5-4, 5, 6 from action in the circuit. Circuit A4 will be reset by CCR to the $\overline{Q}$ state. CCR will also make A5-3 go high and place a reset signal on output line (H). This resets the counters associated with IB2 (118) and IB3 (107). The FF A2 on IB2 will not start counting until INT goes true and unlocks the J and K inputs. The count starts at the start of integration time and when 900 is reached, which is a time interval of one second, inputs 3 and 4 of A4-CC4 (139) go high and A4 goes to the Q state. A low at input 1 of A5 allows A5-3 to go high resetting the buffers. The counters will remain in the zero state and the integrator buffer weights will be set for a one second integration time. The FF A4 can not toggle back because K is inhibited by $\overline{DTS}$. When $\overline{Q}$ of A4 goes low, a high is stored on the output line (T) of the bi-stable circuit A5-8, 9, 10, 11, 12, 13.

In the $\overline{DTS}$ state A5-4, 5, 6 is activated and the K input of A4 is activated. Again, after one second, A4 goes to state Q. Input 1 of A5 goes low and output line (H) goes high resetting the buffer counters. Input 9 of A5 also goes low creating a high at input 5 of A5 after a small delay. This allows A4, 5, 6 to bring output line (H) to a low state where it will be held by A4-5, 6. The counter cycles again after one second and stops at the end of integration. At this time the proper weight is provided for the Integrator buffers. It is possible for the integration to over-run 900 the second time around due to the inhibited reset line, and integration times slightly greater than two seconds can be properly weighted.

4.12 - Description of Driving and Logic Circuitry for X and Y Multipliers and X & Y Demodulators

Block Diagram No. 881-6-01-612

Drive signals for the seven boards for the analog sections of the X and Y Multipliers are shown at the top of diagram 881-6-01-612. This includes signals to XYM1, XM1, XM2, XM3, YM1, YM2, and YM3.

The connections to the 10° step and 10° weight boards of the X multiplier are different than those to the Y Multiplier because the X Multiplier starts from zero and steps to a maximum in a sine manner, whereas, the Y Multiplier starts from maximum and steps to zero in a cosine manner.

The inputs for the .1° STEP GENERATOR are shown in the upper left corner and are created by the XYM 2 board (111). The step generator is stepped as a rising staircase for intervals between 0° to 90° and 180° to 270°. The logic is changed in the remaining areas of 90° to 180° and 270° to 360°, and a falling staircase is produced. Basically the same action takes place for the XM 1 and YM 1 board in the upper right hand corner. They are driven by XYM 5 (111) which is identical to XYM 2 (111). The logic for XYM 2, and XYM 5 is much the same as that for FG 8. Refer to Section 4.3.

The XYM 2 board is driven by the A1 counter on the Readout Board. This is active only during computation time. The counter A1 on board XYM 6 drives the 1° step generator and is active during computation time and integration time.

The XYM 6 (130) board contains a 1° decade counter and a 90° flip flop circuit. In addition it contains a switching circuit that provides Correlator Divided clock pulses to the multipliers during integration time and 1° pulses from the .1° counter during computation time. When the measure cycle is started the CCR signal sets a low on output 3 of A4 of the bi-stable circuit. This makes A3-8 high and correlator DCP pulses are gated from input (T) to output (A) and to the output of A3-6. When state one is reached the bi-stable circuit is set so that A4-3 is high. This gates the pulses on input (L) to output (A) and to the output of 6 of A3. The A and D output of the decade counter A1 are used to provide a negative going pulse at the output 6 of A5 every time 9° is reached. This is gated out to output (C) during $\overline{90°}$ for shift right pulses and to output (F) during 90° for shift left pulses.

The last board required for the multipliers is the 180° and 270° FF board, XYM7 (134). The 180° FF circuit, A2, provides the drive for the X Demodulator at outputs (L) and (M) and the 270° FF circuit, A7, provides the drive for the Y Demodulator at outputs (E) and (H). These FF circuits have to be used in several different ways during a machine cycle as can be anticipated by observing all the logic circuitry

on the board. The logic is all associated with setting and resetting. Assume that the set and reset lines are inactive. Both A2 and A7 are cross coupled and will toggle on a falling edge on inputs (2). The correlator 90° signal goes to input 2 of A2, and therefore, A2 toggles at 0° and 180°. Since the inverse of the 90° signal is fed to input 2 of A7, the 270° FF toggles at 90° and 270°, the two output signals are, therefore, 90 electrical degrees apart as required for sine and cosine multiplication.

Each of the set or reset lines are connected to a number of NAND circuits and when any NAND circuit goes to a short on its output that line will be activated. Any NAND circuit connected to a set or reset line and has a zero on one or both inputs will be inactive as far as setting or resetting a FF circuit.

Consider first the group of circuits, A1 and A6 and A5-8, 9, 10. When the sync pulse on input line (P) goes low A6 is activated by highs at inputs 1, 4, 9 and 13. The output on 3 of A1 will be low when we have (90°) (180° + $\overline{(90°)}$ $\overline{(180°)}$) which will be from 0° to 90° and from 270° to 360°. If the sync pulse should occur in these intervals, A6-8 and A6-6 will go low placing the 180° FF and the 270° FF in the Q state. If the sync pulse should occur from 90° to 180° or 180° to 270°, however, outputs A6-3 and A6-11 will go low and A2 and A7 will be placed in the $\overline{Q}$ state. This part of the logic circuitry is for setting the 180° FF and 270° FF properly immediately prior to the integration period.

The next two logic blocks, A5-11, 12, 13 and A5-4, 5, 6 are used to reverse polarity, by reversing the drive to the X demodulator when the instrument is used in the DVM mode. When input (S) is low indicating DVM not in use, A5-11 and A5-6 will be high and, therefore, inactive. If input (S) is high, however, the two NAND circuits are active and a high at input (R) will place the 180° FF in the Q state and a low at input (R) will place the 180° FF in the $\overline{Q}$ state.

The two FF circuits also have to be set during the comp θ interval and the compute R interval. At A8-8 we have (X+) + (Y+) and at A4-3 we have (X-) + (Y-). There are four possibilities for resetting which are:

$$\overline{Q}_{A7} = \left[(X+) + \overline{(Y+)}\right] \left[\text{COMP R}\right]$$

$$\overline{Q}_{A2} = \left[(X+) + \overline{(Y+)}\right] \left[\text{COMP } \theta\right]$$

$$Q_{A7} = \left[(X-) + \overline{(Y-)}\right] \left[\text{COMP } \theta\right]$$

$$\overline{Q}_{A2} = \left[(X-) + \overline{(Y-)}\right] \left[\text{COMP R}\right]$$

Refer to section 4.1.1 for an explanation of why it is necessary to set the FF's in accordance with the above logic equations.

4.13 - Description of Logic Circuitry for Command Generator, Error Detector, Ramp Generator and DVM Switching Circuit.

Block Diagram No. 881-6-01-613

The description of how the machine operates in the various states from one through eight should be referred to in Section 4.1. The following timing diagram shows the various state signals:

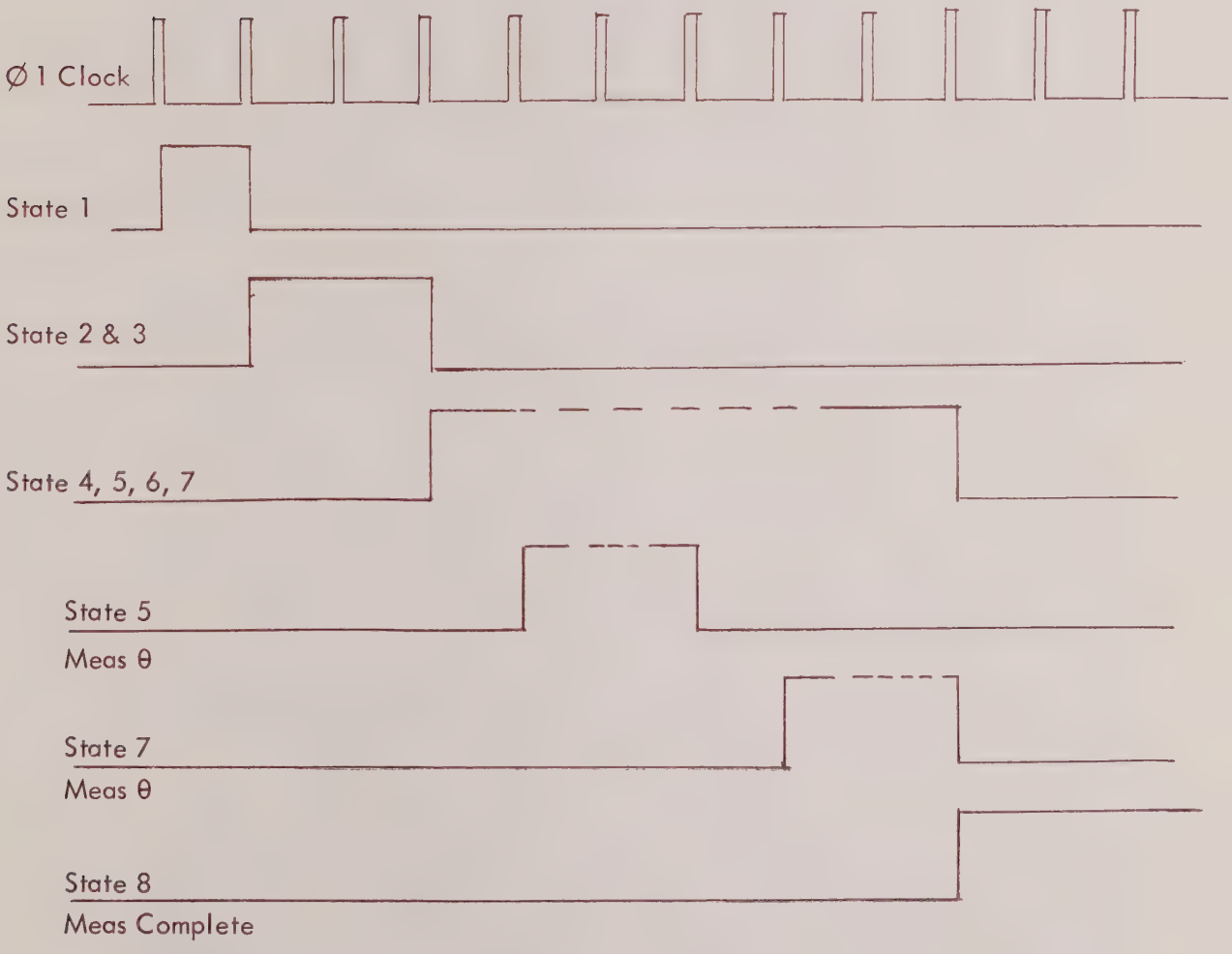


Figure 4.3

The State 5 and State 7 interval are variable in width. The Meas θ interval would have a maximum width equivalent to 899 counts of the $\emptyset_2$ clock (89.9°) and the Meas R interval would have a width equivalent to 1500 counts of the $\emptyset_2$ clock for full scale reading.

The state generator is shown in CC6 (132). It is at rest in state 8 until a new measurement is initiated and the CCR signal resets the outputs of A3 counter to zeros. When the compute time is reached which is

$$\text{Compute} = (\overline{\text{STATE 8}})\ (\overline{\text{INT}})\ (1\ \text{SEC})$$

the first $\emptyset_1$ pulse will put A3 into State 1. Succeeding pulses will put the unit into State 2, 3, 4, 5. When State 5 is reached A6-3 goes low stopping the clock pulses from activating the A3 counter. Another pulse will not put the counter into State 6 until a detect signal (high) appears on input (L). The next pulse will clock the system to state 7 and again the pulse train is inhibited requiring the detect signal on input line (L) to allow the system to go to state 8. The system terminates in state 8 and requires a command chain reset (CCR) to reset the counter to state zero.

The error detect board DVM-2 (126) consists of a comparator circuit and four input switching circuits. Various analog signals are switched into the circuit, compared and when a balance is reached an output detect signal is produced. The detect circuit also is used to determine if a signal is greater or less than zero volts.

The board DVM 1 (123) consists of a precision ramp generator, A1, which is turned on by $\overline{\text{State 7}}$. This command signal appears at input (F). When the signal at output (D) is equal in magnitude to the R signal the Detect signal occurs and the value of R is stored in the Readout register. The ramp generator is also used for DVM. The amplifier A2 is used to sum the signals from the X Multiplier and the Y Multiplier and present the inverted sum to input (D) of DVM-2 (126).

The DVM switching board CC-8 (140) provides the additional circuits necessary to make the machine perform as a digital voltmeter when the front panel mode switch is in the DVM position.

For a detailed description of operation of this board refer to Dwg. CC-8 (140). When input line (L) is grounded DVM operation is initiated. A ground on (L) places a high on A2-11 which in turn puts a high on output line (J). This activates input (R) of DVM-2 (126) which closes circuit No. 4. This applies a signal from the X demodulator which is directly proportional to the D.C. input signal. The polarity may be wrong and this has to be tested for and changed if necessary. How this is done will be explained in a following paragraph.

A high on the output of A2-11 causes A2-8 to go low which removes the drive from Q1. This allows capacitor C2 to charge up to the intrinsic voltage of unijunction transistor Q2. The transistor will fire and short C2 to ground. The transistor recovers and the action repeats itself creating a sawtooth waveform across C2 of about 12 volts peak and .5 to 1 sec. duration depending on the setting of R3. A narrow pulse of .5 to 1 sec. period is created across R5. This pulse triggers the one-shot circuit consisting of Q3 and Q4 and a positive 5 volt pulse of 5 millisecond width and .5 to 1 sec. period is created on the collector of Q5.

If the input signal is positive the error detector output will go positive providing a high at input (H) of CC-8. This allows the $\emptyset_2$ clock to toggle A1 during the 5 ms time that Q5 goes positive. The output (E) of A1 FF will be fed to AJ27-R of XYM-7 and reverse the state of the 180° FF which will reverse the X demodulator.

The NAND circuit A3-1, 2, 3 provides a positive going reset pulse for resetting the R counter at output (M). This will occur whenever a low occurs at input (1) or (2) of A3. A reset pulse will, therefore, be generated when a CCR signal occurs or the 5 ms DVM reset signal occurs.

When output (S) goes low the R counter and Ramp Generator are turned on. The DVM reset pulse causes A4-10 to go low latching A4-8, 9, 10, 4, 5, 6 in a state where A4-8 is high. At the end of the pulse A5-13 also goes high and the measurement starts. When a high occurs at input (H) A4-4 goes low and the bi-stable circuit is reset which makes A5-11 go high, stopping the R counter and Ramp Generator.

4.14 - Description of Operation of Automatic Ranging - Option AR

Drawing No. 881-5-01-621

The purpose of the automatic ranging option is to automatically change the range of the input amplifiers when the input is above or below certain levels. This is accomplished by cycling the instrument through an operation, testing the R reading and allowing the instrument to cycle again if the R reading is above 1600 or below 100. Before re-cycling occurs the range is shifted up if the reading is above 1600 and shifted down if the reading is below 100. If the reading is between 100 and 1600 no change occurs and the unit stops when the state 8 (MEAS COMPLETE) is reached.

The "Partial Wiring Diagram" (881-5-01-621) shows the wiring that controls the Decimal Point Lights and input relays. When the Input Range switch is in the "Auto" position the switch becomes ungrounded and the relays and lights can only be grounded through the transistors on board 881-5-01-138 and 881-5-01-149.

Board No. (149) includes circuitry to decode the electrical settings of the input relays and from this information ground the proper line to the light drives and also to provide a three wire code for remote readout of decimal point according to the following table:

Range	Lines		
	J	M	L
150.0	0	0	+5
15.00	0	+5	0
1.500	0	+5	+5
.1500	+5	0	0

For Board No. (138) the lines S, C, D close the relays for Range 4, Range 3, or Range 1 respectively when they are grounded by Q1, Q2, or Q3. The JK FF's A4 and A6 have four stable states which correspond to the output conditions shown in the following table:

A6		A4		Transistor Closed	Input Range
Q	$\overline{Q}$	Q	$\overline{Q}$		
0	1	0	1	Q1	150 MV
0	1	1	0		1.5V
1	0	0	1	Q2	15V
1	0	1	0	Q3	150V

Three NAND circuits tie points CR1, CR4, CR7 to ground when Auto Range (Line H) is high disabling drive to Q1, Q2, and Q3. When Auto Range is desired, line (H) is grounded and CR1, CR4, and CR7 are ungrounded allowing logic signals to control the relay drive transistors.

The amplitude signals 1000, 800, 400, 200 and 100 are fed to five NAND circuits that are wire-ORed on the output. The output going high indicates the amplitude is less than 100. Likewise if the output of A2-3 goes high the amplitude is greater than 1600. The "In Range" signal at output (J) will go high if the R reading lies between 100 and 1600. If the R reading is out of range, the input signal (State 8) is enabled and the rising edge toggles the A4-A3 circuit to a new state. The instrument will keep cycling until an "In Range" signal is received.

To aid with the understanding of circuit operation, a Timing Diagram is shown on page 4.37, Fig. 4.7.

4.15 - Description of Operation of Remote Read Out - Option P

Drawing No. 881-5-01-623

The Remote Readout Option for the basic instrument allows the front panel data to be presented to an output connector. This data is in Parallel BCD Format working between 0 and +5 volts using DTL logic with capability of positive or negative logic.

The details of the wiring to the back connector are shown on drawing (881-5-01-623). The phase and amplitude signals route down to buffer boards E1 and E2 (Dwg. No. 881-5-01-150-0) and then to output connector J105.As an example, consider the lines .1°, .2°, .4° and .8° going to E1-A1. These signals are impressed upon inputs A, B, C, D of A1 respectively. There is no inversion and the same signals appear at outputs A, B, C, D of A1 when the strobe input is reduced to zero from the +5V level.

Blocks A2, A3, A4, and A5 are isolating and inverting blocks. If the phasing line is grounded the output signals on lines A31, A32, A29, and A35 will be inversions of inputs on B33, B34, B32, and B31. This can be seen in detail by referring to Dwg. No. 881-5-01-150. The above description fits the 16 circuits located on boards E1 and E2.

A binary coded signal for the decimal point is available from the Auto-Decimal Light Driver. (881-5-01-149) so this board is provided to supply the necessary signals at E2-B25, E2-B28, and E2-B27.

The strobe generator and two isolating circuits for "Meas Complete" and "Meas Complete and In Range" are provided on the board located in card space AJ28. By means of "Schematic, Strobe Circuit" Dwg. No. (155) and the timing diagram (Fig. No. 4.7) it can be seen how a negative going strobe signal is generated for E1 and E2. This signal occurs during State 8 (Meas Complete) and instantaneously puts a new number on the output lines after each measurement cycle is completed.

The wiring and usage of boards E1 and E2 are identical for the Type F Option. Basically four more boards E3, E4, E5, and E6 plus additional wiring to the front panel, and 3 front panel relays are needed for the Type F Option.

4.16 - Description of Operation of Remote Programming - Option F

Drawing No. 881-5-01-621, 881-6-01-622, 881-6-01-623

The Type F Option instrument includes the Type P and Type AR circuitry so the above drawings plus Sections 4.14 and 4.15 should be read when studying this section as this data is not repeated here.

The additional boards needed to provide for input command signals are shown schematically on Dwg. No. (622) with necessary inter-wiring and wiring to a separate input command cable connector.

A description of the operation for input commands is as follows: For the boards E5 and E6 take lines 1F, 2F, 4F, 8F as an example. If voltages are applied to lines B33, B34, B32, and B35 and the strobe line is dropped from +5V to 0V the data will be transferred to A1 - 5, 9, 2, 12 outputs. If the phasing line is high, the outputs on A, B, C, D will be transferred without change, but if the phasing line is low the complement will appear on lines A31, A32, A29, A35. All 16 circuits on E5 and E6 operate in this same manner.

Consider next the signals 1F through 800F and take 1F as an example. When 1F is selected E4-A31 goes low allowing E4-A32 to go high which is an activating signal for the oscillator. If local operation is in effect the outputs from E5 and E6 will be high and switch S1 will be grounded. If S1-B1 is ground, for example, E4 B31 will be low and output E4-A32 will again be high. In local operation, grounding the twelve switch lines as desired in a BCD manner will activate the desired oscillator frequency. Likewise, if the switch sections are ungrounded, the lines from E5 can be grounded in a BCD manner to select the desired frequency remotely.

For ranging, the desired range line is activated and the outputs from E5 which are A12, A13, A10, A16 ground the desired line CJ8 (N, P, R, S) which activates the selected range. In local operation E5-A12, A13, A10, A16 remain high and outputs E4-A15, A14, A13, A16 ground the desired line. This action is created by switch S1, Section A.

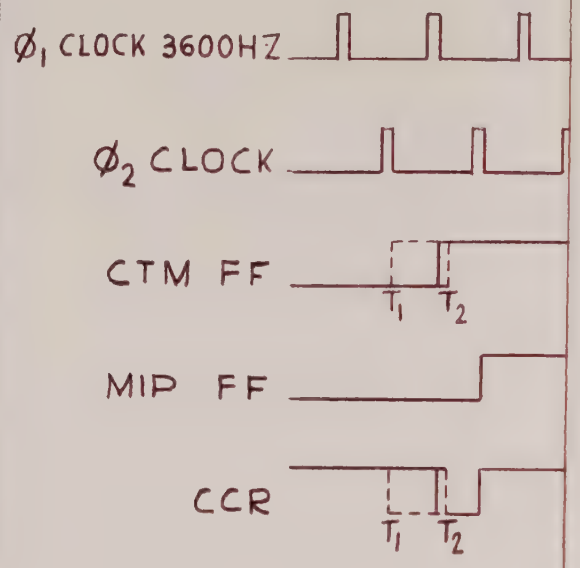
In a similar manner, for remote command of output amplitude, when input lines E5-B7, B10, B9, B11; E5-B3, B4, B2, B5; E6-B33 are activated and strobed into the registers the complement will appear on E5, E6 output lines. These lines are fed to relay board E3 and a zero on any input will result in a relay closure on the Remote Program Board 0A1 (AJ1). A relay closure can be checked by observing if the corresponding output line E3-B2, B3, B1, A1, B8, B9, B12, A7, B14 is at ground potential.

Input Ranging signals enter E6 board on B25, B28, B27 and B29 and are strobed in by B36. These signals are fed to points CJ20H, CJ20J, and CJ20L as shown. In remote operation the wiper of S4A is ungrounded and the proper line H, J, or L must be grounded by the remote cable.

The next set of signals entering A11 on Board E6 are Carrier Demodulator In, DC-AC, and sine wave - square wave. To use the instrument in carrier mode, the demodulator would be energized; DC-AC would be on AC and the sine wave mode would be used. These signals enter E6 on B21, B22, B20 and exit on A19, A22, A21. They enter the relay driver board E3 on B25, A21, B29, respectively and exit on B23, B19, B27. The point B27 drives relay K1 which places either a sine or square wave on output potentiometer R4.

For the rest of the control signals it can be seen that for a high signal at the inputs, a ground signal is produced at CJ20F for Measure; CJ20S for X10 Int; CJ9-B for Stop 0; CJ9-A for Stop 90; and CJ8J for 0° - 180°.

REVISION	BY	CHK.	APP.	DATE



B

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881-6-01-001	1410
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APPLICATION	

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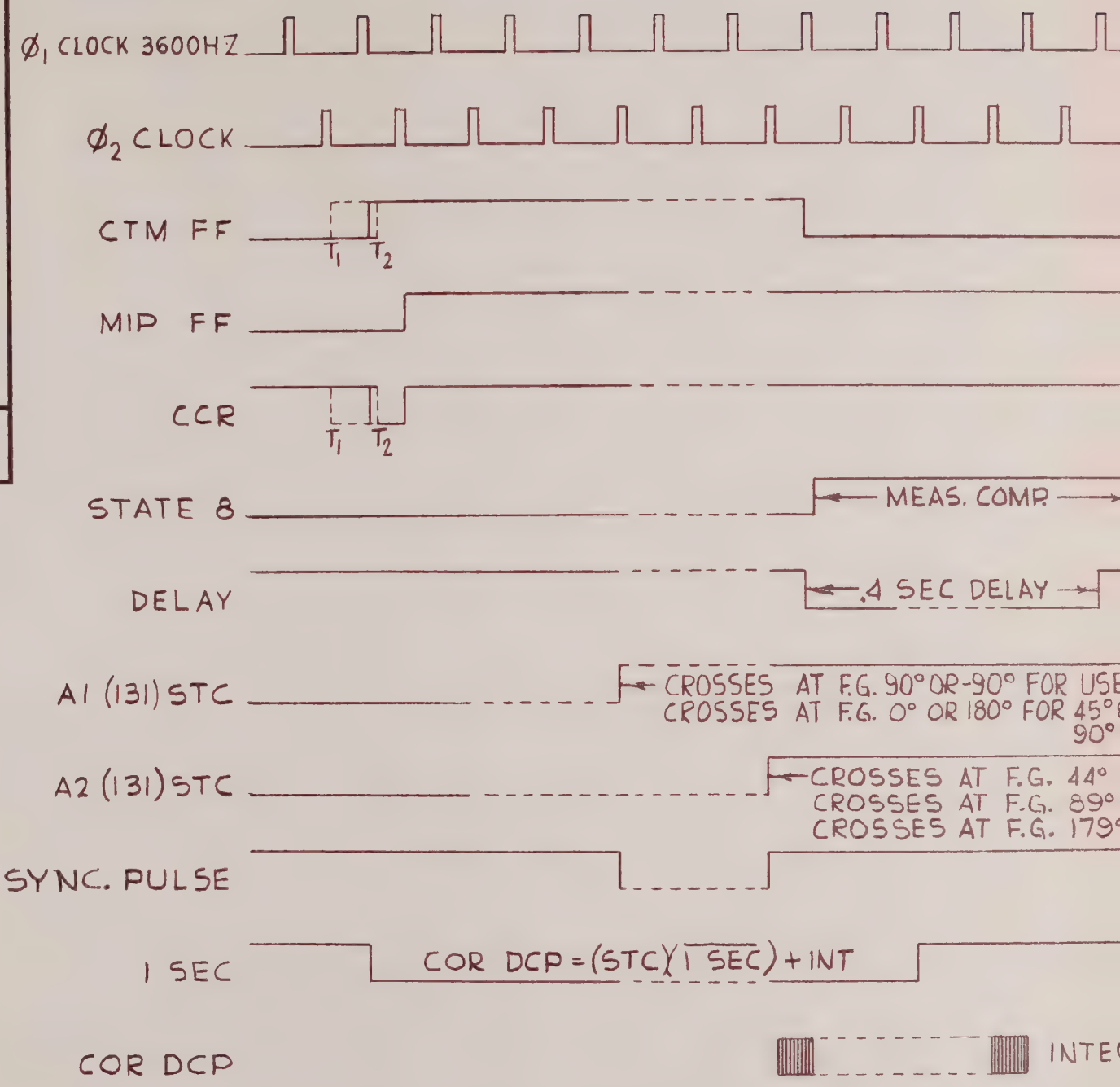
881-3-01-074	0
SCALE 1/4	SECTION 4 PG 34

DWG. REV.



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			DR. T. SMITH	THREE DEC. PLCS. ±.005 TWO DEC. PLCS. ±.010 FRACTIONS ±1/64 ANGLES ±0° 30'
			CHK.	
			APP. DEKOT	
881-6-01-001	1410		APP.	
NEXT ASSY.	USED ON		MATL.	FINISH
APPLICATION				

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R 45°
R 90°
OR USE

ATE ENDS

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TIMING DIAGRAM FOR CC1(144) & CC2(131) FIG. 4.4

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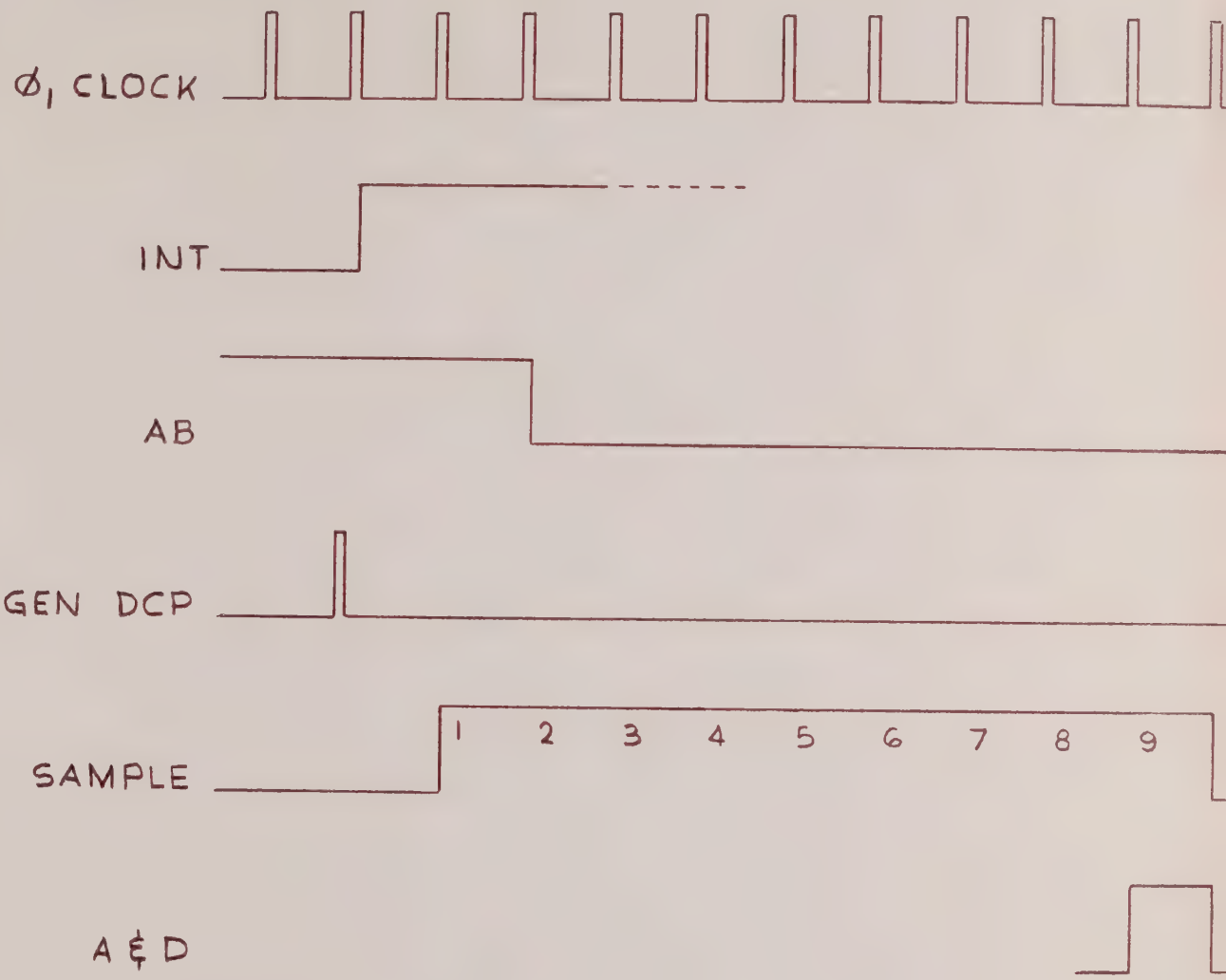
DWG. SIZE			DWG. REV.
B	881-3-01-074		0
	SCALE 1/4	SECTION 4 PG 34	



B

881-6-01-001	1410
NEXT ASSY.	USED ON
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DR. T. SMITH
CHK. H. Flowers
APP. D. E. Kitts
APP.
MATL.

UNSPECIFIED TOLERANCE

THREE DEC. PLCS. ±.005
TWO DEC. PLCS. ±.010
FRACTIONS ±1/64
ANGLES ±0° 30'

FINISH

NO.	REVISION	BY	CHK.	APP.	DATE

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TIMING DIAGRAM FOR CC3(133)

FIG. 4.5

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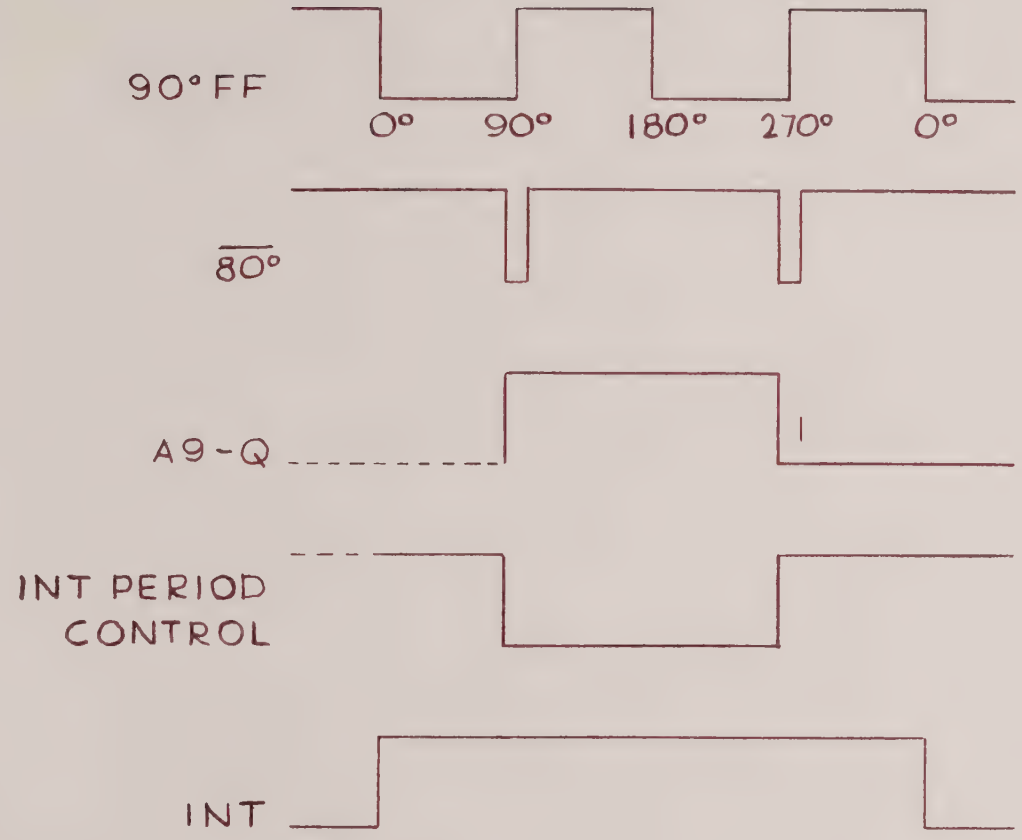
DWG. SIZE		DWG. NO.	DWG. REV.
B	881-3-01-072		O
	SCALE NH	SECTION 4 PG. 35	



A

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TIMING DIAGRAM FOR CC4(143) FIG. 4.6

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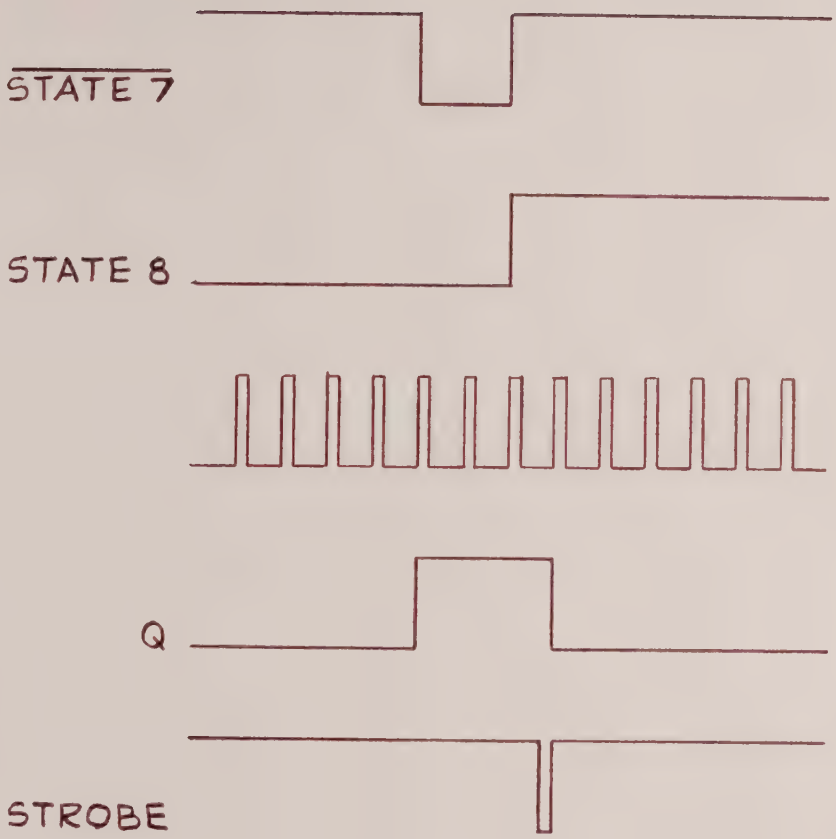
CHK. H N Flem		
APP. D E Kutas		
APP.		
MATL.	881-6-01-001	1410
FIN.	NEXT ASSY	USED ON

EMR HATBORO

EMR DIVISION OF WESTON INSTRUMENTS, INC

A SCHLUMBERGER COMPANY

A	881-2-01-070		O
DWG. SIZE	SCALE ~H	SECTION 4 PG 36	DWG. REV.



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TIMING DIAGRAM
STROBE CIRCUIT FIG. 4.7

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APP.		
APP.		
MATL.	881-6-01-001	1410
FIN.	NEXT ASSY	USED ON

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

A	881-2-01-071		O
DWG. SIZE	SCALE	SECTION 4 PG. 37	DWG. REV.

5 - MAINTENANCE

5.1 - Performance Verification Test

NOTE

IF THIS INSTRUMENT PERFORMS WITHIN THE STATED LIMITS AS SET OUT IN THE FOLLOWING PERFORMANCE VERIFICATION TEST, YOUR INSTRUMENT IS PERFORMING ACCORDING TO ITS SPECIFICATIONS. THERE IS THEREFORE NO REASON FOR ADJUSTMENT OR CALIBRATION.

5 - MAINTENANCE

5.1 - Performance Verification Test

5.1.1 - Equipment Required

DVM (AC and DC), capable of 0.1 mv resolution.

Distortion Analyzer, hp 331 A or equivalent.

Counter, Weston Model 2052 or equivalent.

Oscillator (Audio Range), hp 200 CD or equivalent.

Oscilloscope, Tektronix 515 A or equivalent.

5.1.2 - General

The following control settings are to be used as a reference point. Any deviation from these settings will be noted with the instructions for a particular measurement. The state of the correlator after power is first applied, is indeterminate and for this reason, MEASURE-SGL should always be initiated after applying power.

Basic Settings

FUNCTION	DC Sine Wave
STOP	Center-Off Position
BIAS	Center-Off Position
BIAS LEVEL	Counter-Clockwise
PHASE	0°
AMPL	0 - 15 v
OUTPUT	Clockwise
FREQUENCY/HZ	1000×10^{-1}
INT	X1
LEAD	0° (Center Position)
DEMOD	OUT
LEVEL	Counter-clockwise
MEASURE	Center-Off Psoition
INPUT RANGE	15
DC REJECT	OFF
MODE	R θ

NOTE: For these tests the metal shorting links supplied with instrument should be in place (for single ended operation) between the LO input and SIG GND; and between SIG GND and chassis.

5.1.3 - Evaluation

A - Connect the HI input jack to the OUTPUT jack.
Connect a DVM (DC) to the OUTPUT jack.

Use Basic Settings Except:

Change MODE to DVM

Change STOP to 90°

Read (ext. DVM) _____v, 15.00 min.

After recording the first reading, adjust the OUTPUT Amplitude control for a reading of 15.00. The dial can now be locked because the amplitude will not need to be readjusted for the remainder of the performance test.

Read (int. DVM) _____v, 15.00 ±.15

Change PHASE to 180° Read (ext. DVM) _____ v, -15.00 ±.08

Read (int. DVM) _____v, -15.00 ±.15

B - Same connections as above.

Use Basic Settings Except:

Change MODE to DVM

Change STOP to 0°

Change INPUT RANGE to .15

Change PHASE to 0° Read (ext. DVM) _____v, -0.120 ±.030

Read (int. DVM) _____v. -0.120 ±.030

Change PHASE to 180° Read (ext. DVM) _____v, 0.120 ±.030

Read (int. DVM) _____ v, 0.120 ±.030

Change BIAS to (+)

Change INPUT RANGE to 15

Set BIAS LEVEL Clockwise Read (ext. DVM)_____v, +10.00 min.

Read (int. DVM) _____ v, +10.00, min.

Change PHASE to 0°

Change BIAS to (-) Read (ext. DVM) _____v, -10.00 min.

Read (int. DVM) _____v, -10.00, min.

Change BIAS to Center-Off Position

Change INPUT RANGE to 150

Change DC REJECT to (+)

Set LEVEL Clockwise Read (int. DVM) ____v, -99.0 MIN

Change DC REJECT to (-) Read (int. DVM) ____v, +99.0 MIN

C - Change external DVM to AC Measurement

Return to Basic Settings:

Read (ext. DVM) ____v rms, 10.5 min.

Change AMPL to 0 -1.5 v Read (ext. DVM) ____v rms, 1.05 min.

D - Connect the distortion analyzer and oscilloscope to the OUTPUT jacks.

Use Basic Settings Except:

FREQUENCY/HZ 1000 X10^{-2} Read ____%, 1% max. Distortion

1000 X10^{-0} Read ____%, 1% max. Distortion

E - Connect the counter to the OUTPUT jacks.

Use Basic Settings Except:

Change FUNCTION to DC Square Wave

Change FREQ/HZ to 1000 X10^{-1} Read ____ Hz, 100.00 ±0.5%

9990 X10^{-2} Read ____ Hz, 99.90 ±05%

9990 X10^{-0} Read ____ Hz, 9990 ±0.5%

Change the counter to period measurement.

Set FREQ/HZ 0010 X10^{-3} Read ____msec. 100,000 ±0.5%

F - Make certain the HI input jack is still connected to the OUTPUT jack. Activate the MEASURE-SGL switch for each of the following settings of the controls.

	R	θ	
Use Basic Settings	_____	_____	
LEAD to 45°	_____	_____	
LEAD to 90°	_____	_____	15.00 v ±.15
PHASE to 180°	_____	_____	and
LEAD to 45°	_____	_____	Selected Phase ±0.5°
LEAD to 0° (Center Pos)	_____	_____	
Use Basic Settings Except:			
FREQ/HZ 9990 $X10^{-1}$	_____	_____	
LEAD to 45°	_____	_____	15.00 v ±.15
LEAD to 90°	_____	_____	and
PHASE to 180°	_____	_____	Selected Phase ±0.5°
LEAD to 45°	_____	_____	
LEAD to 0° (Center Pos)	_____	_____	
Use Basic Settings except:			
FREQ/HZ 100 $X10^{-4}$	_____	_____	
LEAD to 45°	_____	_____	15.00 v ±.15
LEAD to 90°	_____	_____	and
PHASE to 180°	_____	_____	Selected Phase ±0.5°
LEAD to 45°	_____	_____	
LEAD to 0° (Center Pos)	_____	_____	
Use Basic Settings Except:			
FREQ/HZ to 9990 $X10^{-1}$			
INPUT RANGE to 150	_____	_____	
LEAD to 45°	_____	_____	015.0 v ±0.5
LEAD to 90°	_____	_____	and
PHASE to 180°	_____	_____	Selected Phase ±1.0°
LEAD to 45°	_____	_____	
LEAD to 0° (Center)	_____	_____	

G - Connect the HI input jack to the OUTPUT jack. Connect an oscillator to the CARRIER input jack.

Use Basic Settings
Except:

Change STOP to 90°

Change FUNCTION to AC Sine Wave

Change DEMOD to IN

Change FREQUENCY/HZ to 9000 $X10^{-2}$

Inject 1000 Hz at 15 v rms into the CARRIER INPUT and adjust the carrier LEVEL for 10.61 v rms at the OUTPUT jacks.

	R	θ	
Change STOP to Center-Off Pos			
Change MEASURE to SGL	_____	_____	15.00 ±.15
Change PHASE to 180°			and
Change MEASURE to SGL	_____	_____	Selected Phase ±1.0°

5.1.4 - Option F, Remote Readout Evaluation

A. Set up basic switch settings listed in Paragraph 5.1.2. Set the output logic switch to the POS. position (on rear panel). Change phase from basic setting to 180° position and depress the SGL. (single) side of the measure switch.

Sample readout of front panel display
R = 15.00, O = 179.9 LEAD light out

The table below shows the remote readout for the above reading. (Pins indicated are located on J105).

R

1	5	.O	O
$\overline{E}$	$\overline{A}$ $\overline{B}$ $\overline{C}$ $\overline{D}$	W X Y Z	S T U V
+5	+5 0 +5 0	0 0 0 0	0 0 0 0

θ

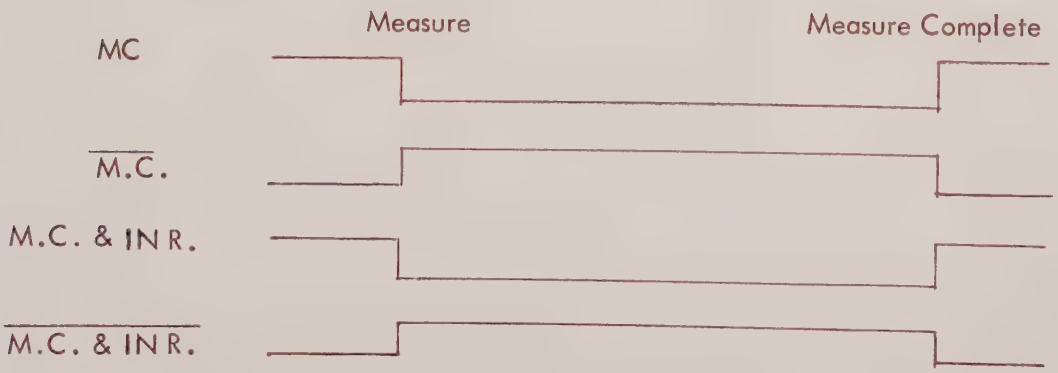
1	7	9	.9
P	K L M N	E F H J	A B C D
+5	+5 +5 +5 0	+5 0 0 +5	+5 0 0 +5

F

1000	100	10	Mult.
1 2 4 8	1 2 4 8	1 2 4 8	10^{-0} 10^{-1} 10^{-2} 10^{-3}
$\overline{Y}$ $\overline{Z}$ AA BB	$\overline{U}$ $\overline{V}$ $\overline{W}$ $\overline{X}$	$\overline{P}$ $\overline{R}$ $\overline{S}$ $\overline{T}$	CC DD EE FF
+5 0 0 0	0 0 0 0	0 0 0 0	0 +5 0 0

Lead	Dec. 1 2 4
R	$\overline{F}$ $\overline{H}$ $\overline{J}$
0	0 +5 0

Read Commands



B. Slide the Output Logic Switch to the COMPL. Position and repeat the same measurement taken in 5, 1, 4-A.

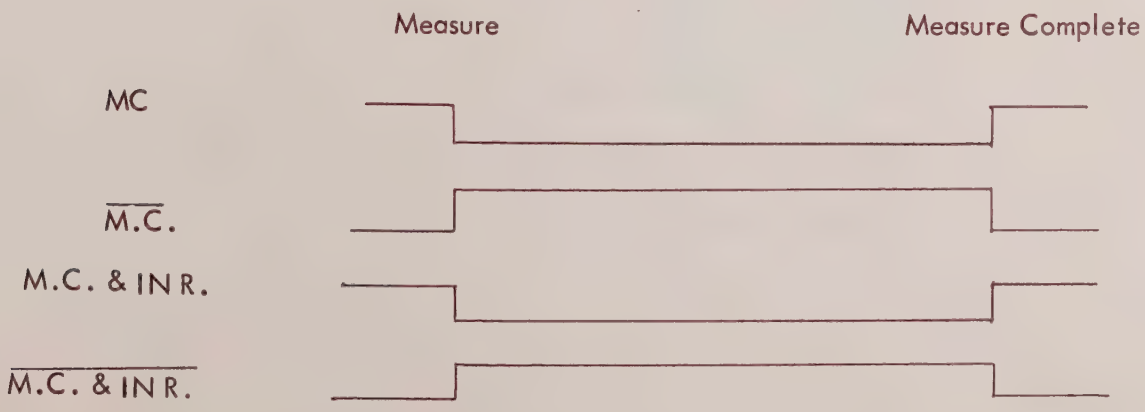
Sample readout of front panel display, R = 15.00, θ = 179.9 LEAD light out

The table below shows the remote readout for the above reading. (pins indicated are located on J105)

$\overline{1}$ $\overline{E}$ 0	$\overline{5}$ $\overline{A}$ $\overline{B}$ $\overline{C}$ $\overline{D}$ 0 +5 0 +5	.0 W X Y $\overline{Z}$ +5 +5 +5 +5	0 S T U V +5 +5 +5 +5
1 P 0	7 K L M N 0 0 0 +5	9 E F H J 0 +5 +5 0	.9 A B C D 0 +5 +5 0
1000	100	10	Mult.
$\overline{1}$ $\overline{2}$ 4 8 $\overline{Y}$ $\overline{Z}$ AA BB 0 +5 +5 +5	$\overline{1}$ $\overline{2}$ $\overline{4}$ $\overline{8}$ $\overline{U}$ $\overline{V}$ $\overline{W}$ $\overline{X}$ +5 +5 +5 +5	$\overline{1}$ $\overline{2}$ $\overline{4}$ $\overline{8}$ $\overline{P}$ $\overline{R}$ $\overline{S}$ $\overline{T}$ +5 +5 +5 +5	10^{-0} 10^{-1} 10^{-2} 10^{-3} CC DD EE FF +5 0 +5 +5

Lead R +5	Dec $\overline{1}$ $\overline{2}$ 4 $\overline{F}$ $\overline{H}$ $\overline{J}$ +5 0 +5

Read Commands



5.1.5 - Option F, Remote Programming Evaluation

A. Refer to Section 2.9, Input Signal Chart, for pin designations to wire programmer to the 1410.

B. Program the following information to be true in accordance with the procedure stated in Section 3.6 for the command lines listed on the input signal chart, Fig. 2, Section 2.9.

Rear Panel

Input Logic Sw. -	POS.
Remote - Manual Sw. -	REMOTE

Front Panel

Bias -	Center - Off Position
DC Reject -	OFF

Connect Generator Output to Correlator Hi Input with a wire

Connector Signals

Strobe Lines -	False (4V ±1V)
Ampl. -	15V
Freq. -	1000 Hz
Freq. Mult. -	10^{-1}
Input Range -	15V

All other lines false

C. Ground all strobe lines and put a true signal on the measure line.

The instrument should now be continuously reading out 15.00 volts and 000.0° ± specification. The generator frequency should be 100 Hz.

Without interfering with the data lines put a false command (4V ±1V) on all the strobe lines.

Now change the following commands:

Ampl -	1.5V
Freq. -	2000V
Freq. Mult. -	10^{-2}

All other lines false, except measure.

The instrument should still be reading out 15.00 and 000.0°.

Ground all strobe lines

The readout should now be 1.500 volts and 000.0° ± specification. The Generator frequency should be 20 Hz.

D. Repeat steps B and C except put the Input Logic Switch (rear panel) in the COMPL. Position.

5.1.6 - Options AR and F Auto Ranging Evaluation

(If the instrument has a F Option put the remote manual switch on the rear panel in the Manual Position).

Set the Front Panel Controls to the basic settings listed in Section 5.1.2.

Put the input range switch in the Auto position and vary the Output Amplitude Potentiometer down to 90 MV and back to 15V. The range should shift down to a smaller range when the reading is below 0100 or up to a larger range when the reading is above 1600.

5.2 - INSTRUMENT CIRCUIT ACCESS

5.2.1 - Cover Removal

Each of the two covers, top and bottom, is held in place by two screws. Remove the two screws, located at the front corners, and lift the front edge of the cover slightly. Apply pressure against the front edge to slide the cover toward the rear of the instrument. A side-to-side rocking motion while applying pressure simplifies removal. Approximately one half inch of travel is required to unlock the rear edge of the cover from the chassis frame.

NOTE

CALIBRATION PROCEDURES SHOULD NOT BE UNDERTAKEN UNLESS THE INSTRUMENT HAS FAILED THE PERFORMANCE VERIFICATION TEST IN SECTIONS 5.1.1 THROUGH 5.1.6.

5.3 - Calibration Procedure

5.3.1 - General

Sequence is important. At any time an adjustment is made, subsequent steps may have been affected and should be checked. For the same reason, power supply voltages should not be re-adjusted once calibration of the instrument has begun.

When zeroing amplifiers, levels of less than 1 mv should be attained with the exception of those adjustments where an approximate zero is asked. These exceptions normally involve the adjustment of open loop amplifier and readings of less than 1 v are acceptable. After adjustment is made, voltage will vary considerably in either direction - it is not cause for concern. When applying a ground in the calibration process, use the closest pin K.

5.3.2 - Equipment Required

Oscilloscope, Tektronix 515 A or equivalent.

Distortion Analyzer, hp 331 A or equivalent.

Counter, Weston Model 2052 or equivalent.

Digital Voltmeter, capable of 0.1 mv resolution, Weston Model 1420 or equivalent.

AC Voltmeter, hp 3440 A with 3445 plug-in or equivalent.

Oscillator (Audio Frequencies), hp 200 CD or equivalent.

5.3.3 - DA 1410 Generator

A - Verify the power supply voltages, +20 VDC and -20 VDC which can be found at TP1 and TP2 respectively on power supply board No. 881-5-01-222. +5 VDC can be checked at the test point on board No. 881-5-01-247.

B - Front Panel Conditions

FUNCTION	DC Sine Wave
STOP	Center-Off Position
BIAS	Center-Off Position
BIAS LEVEL	Counter-Clockwise
PHASE	0°
AMPLITUDE	0-15v

OUTPUT	Clockwise
FREQUENCY/HZ	1000×10^{-1}

C - Preliminary Adjustment

a) Connect a DVM to board CJ2, pin S (CJ2-S)

b) Adjust ZERO ADJ. (Front panel, right side) for zero volts within ±50 mv.

D - Master Oscillator Frequency Adjustment

a) Place scope probe in TP1 of CJ5.

b) The observed pulses should be at approximately 3600 pulses per second, and should not visibly vary as the most significant digit on the frequency selector is changed in either direction.

c) Return FREQUENCY/HZ to 1000×10^{-1}.

d) Change FUNCTION to Square Wave.

e) Connect counter to OUTPUT.

f) Adjust R13 on CJ3 for 100 cycles per second on the counter.

g) Return FUNCTION to Sine Wave

E - Summing Amplifier Zero Adjustment

a) Ground BJ1-R.

b) Connect the DVM probe to TP2 on BJ1.

c) Adjust R5 for approximately zero volts. (Refer to general comments on page 5-12, paragraph 5.3.1)

d) Remove ground from BJ1-R.

F - Output Amplifier Zero Adjustment

a) Connect the DVM probe to the test point on CJ2.

b) Remove BJ1 and ground CJ2-M.

c) Adjust R7 on CJ2 for approximately zero volts on the DVM.

d) Remove ground from CJ2-M and ground CJ2-R.

e) Adjust R16 on CJ2 for zero volts.

f) Remove ground and replace BJ1.

G - Reference Amplifier Adjustment

a) Place STOP switch in 90° position.

b) Connect the DVM probe to the OUTPUT jack.

c) Adjust R4 on BJ5 for +15.00 volts on the DVM.

d) Place PHASE switch in 180° position.

e) Adjust R5 on BJ5 for -15.00 volts on the DVM.

f) Return PHASE switch to 0° position and STOP switch to center-off position.

H - Zero Adjustment of 1° Generator

a) Remove BJ5 and ground BJ4-E.

b) Connect the DVM probe to the test point on BJ4.

c) Adjust R9 on BJ4 for zero volts.

d) Remove ground from BJ4-E and replace BJ5.

I - Gain Adjustment of 1° Generator

a) Connect the distortion analyzer to OUTPUT jack.

b) Adjust R13 on BJ4 for minimum distortion (approximately 0.5%.

5.3.4 - DA 1410 Correlator

A - Front Panel Conditions

FUNCTION	DC Sine Wave
STOP	Center-Off Position
BIAS	Center-Off Position
PHASE	0°

AMPL	0-15V
OUTPUT	Clockwise
FREQUENCY/HZ	1000×10^{-2}
INT	X1
LEAD	Center-Off Position
DEMOD	OUT
LEVEL	Counter-Clockwise
MEASURE	Center-Off Position
INPUT RANGE	.15
DC REJECT	OFF
MODE	R 0

B - Preliminary Adjustment

a) Connect a DVM to CJ20-P.

b) Adjust ZERO ADJ (front panel, left side) for zero volts.

c) On CJ12, connect a DVM to pin 4 of A1.

d) See that the instrument is indicating MEAS COMPL and adjust R13 on CJ12 for zero volts on the DVM.

C - Input Amplifier Offsets

a) Ground the input jacks and select the 150V input range.

b) Adjust R6 on CJ24 for zero volts on the summing buss - accessible at the junction of R14 and C10.

c) Adjust R6 on CJ28 in the same manner.

d) Select the 1.5V range.

e) Adjust R17 on CJ24 for zero volts on CJ24 test point.

f) Adjust R17 on CJ28 for zero volts on CJ28 test point.

g) Repeat above if necessary because of interaction.

D - Mixer Amplifier Offset

a) Remove CJ24 and CJ28.

b) Ground CJ25-R and CJ25-S.

c) Adjust R7 for zero volts at CJ25 test point.

d) Remove grounds and replace CJ24 and CJ28.

E - Synchronous Demodulator Offset Adjustment

a) Remove AJ27 and CJ25.

b) Ground CJ18-R.

c) Connect a DVM to the test point on CJ21.

d) Ground CJ21-M and adjust R25 on CJ21 for zero volts.

e) Unground CJ21-M, ground CJ21-L and adjust R15 on CJ21 for zero volts.

f) Repeat steps d) and e) if necessary.

g) Repeat steps c), d), e), and f) on CJ22.

h) Remove grounds and replace CJ25.

i) Remove ground from HI input jack.

F - Synchronous Demodulator Gain Adjustment

a) Leave AJ27 out and phase input range switch in 15v.

b) Connect the HI input jack to OUTPUT jack and place the GENERATOR in the STOP 90° position.

c) Connect a DVM to the test point on CJ21,.

d) Ground CJ21-L and observe the DVM reading (approximate 2.4 v)

e) Remove the ground from CJ21-L, ground CJ21-M and adjust R21 on CJ21 to match the reading observed in step d), except for polarity.

f) Follow steps c), d), and e) in adjusting CJ22.

g) Remove the grounds and replace AJ27.

G - Correlator Summing Amplifier Adjustment

a) Connect a DVM to the BJ19 test point and ground BJ19-R.

b) Adjust R5 on BJ19 for approximately zero volts. (Refer to general comments on page 5-12, paragraph 5.3.1)

c) Apply step a) and b) to BJ26.

d) Remove grounds.

H - One Degree Generator Zero Adjust

a) Remove CJ21 and ground CJ21-R.

b) Connect a DVM to the BJ15 test point.

c) Adjust R9 on BJ15 for zero volts.

d) Remove the ground, replace CJ21 and move the DVM to the BJ22 test point.

e) Remove CJ22 and ground CJ22-R.

f) Adjust R9 on BJ22 for zero volts.

g) Remove the ground and replace CJ22.

I - X ± Y Summing Amplifier Adjustment

a) Remove BJ19 and BJ26.

b) Ground CJ11-P and CJ11-N.

c) Connect a DVM to CJ11-M.

d) Adjust R-20 on CJ11 for zero volts.

e) Remove grounds and replace BJ19 and BJ26.

J - Integrator Zero Adjust

a) Place STOP switch in center-off position.

b) Initiate a single measurement and wait for MEAS COMPL to light.

c) Connect a DVM to the BJ21 test point.

d) Adjust R24 on BJ21 for zero volts.

e) Move the DVM probe to the BJ28 test point.

f) Adjust R24 on BJ28 for zero volts.

K - Integrator Buffer Zero Adjustments

a) Remove BJ21.

b) Connect a DVM to the CJ16 test point.

c) Ground CJ16-B and adjust R16 (V-Bal) on CJ16 for approximately zero volts.

RAMP ZERO ADJUST - ADDITIONAL EXPLANATION

The purpose of this adjustment is to set the reference threshold of a comparator. At threshold the output of a comparator is logically indecisive. This is the indicator used in this step and it is desired that a signal be seen which alternates erratically between the two logic levels. Some DC voltmeters will average this fluctuating signal to between one and two volts; some newer and faster ones will not. Also, since the adjustment is so sensitive, the output will 'choose' one state or the other as soon as adjustment has been completed. This will not affect the accuracy of the calibration.

d) Remove ground from CJ16-B, ground CJ16-D and adjust R-19 (C-Bal) on CJ16 for zero volts.

e) Repeat steps c), and d) if necessary.

f) Remove grounds and replace BJ21.

g) Move DVM probe to the CJ17 test point.

h) Remove BJ28.

i) Ground CJ17-B and adjust R16 (V-Bal) on CJ17 for approximately zero volts.

j) Remove ground from CJ17-B, ground CJ17-D and adjust R19 (C-Bal) on CJ17 for zero volts.

k) Repeat steps i) and j) if necessary.

l) Remove grounds and replace BJ28.

Error Detect Bias Adjustment

NOTE: Not present on earlier models.

a) Make a single R & θ measurement.

b) On CJ12, connect a DVM to A1 pin 4.

c) Adjust R13 for a reading of zero volts.

L - Ramp Zero Adjust

a) Select DVM on MODE switch.

b) Remove CJ21 and ground CJ21-R.

c) Connect a DVM to CJ12-C.

d) Adjust R11 on C11 for a reading between 1v and 2v. NOTE: This is not actually a DC voltage but a point of instability between logic levels. If preferred, this instability can be observed as erratic switching by using an oscilloscope.

e) Remove the ground and replace CJ21.

M - Ramp Slope Adjustment

a) Select DVM on the MODE switch.

b) Place STOP switch in 90° position and set OUTPUT clockwise

c) Connect an external DVM to the OUTPUT jack.

d) Adjust R3 on CJ11 so that the reading of the internal DVM agrees with that of the external DVM.

N - Display Time Adjustment

a) Connect scope probe to BJ13-S.

b) Still in DVM operation, adjust R3 on BJ13 such that the signal on the scope is approximately ground for one-half second.

O - Gain Adjustment of 1° Steps

a) Set the controls as follows:

STOP	Center-Off Position
FUNCTION	DC Square Wave
FREQUENCY/HZ	1000×10^{-1}
INT	X10
LEAD	0°
MEASURE	SGL
MODE	CAL

b) Connect the scope probe to the BJ19 test point. A full-wave rectified sine wave should now be visible on the scope. For best presentation, synchronize to the signal at the OUTPUT jack.

c) Increase the vertical and horizontal sensitivity of the scope until the 1° steps are clearly visible (0.1 v/cm and 0.1 m sec/cm). Adjust R13 on BJ15 for uniform steps. During adjustment variation will be noticeable at the step that carries the 10° step transient.

d) Change LEAD to 90°, and move the scope probe to the BJ26 test point.

e) Adjust R13 on BJ22 as in step c).

P - Integrator Buffer Gain and Linearity Adjustment

a) Set the Controls as Follows:

FUNCTION	DC Sine Wave
STOP	Center-Off Position
BIAS	Center-Off Position

AMPL	0-15V
OUTPUT	Clockwise
INT	X1
LEAD	0° (Center Position)
DEMOD	OUT
MEASURE	RPT
INPUT RANGE	15 V
DC REJECT	OFF
MODE	Rθ

b) Set FREQUENCY/HZ to 5200 $X10^{-4}$

c) Adjust R24 (gain) on CJ16 until the readout is 8 to to 10 digits higher than the DVM reading from Ramp slope adjustment.

d) Set FREQUENCY/HZ to 5200 $X10^{-2}$

e) Adjust R2 (LIN) on CJ16 to agree with reading in step c) above.

f) Select 180° on PHASE switch. If reading differs from that obtained in 0° PHASE, readjust so that the actual readings are spaced symmetrically about the desired reading.

g) Repeat Steps b), c), d) and e) until the effects of interaction become negligible.

h) Set LEAD to 90° and repeat the above process (steps b) through g) on board CJ17.

Q - Integrator Drift Adjustment

a) Place LEAD switch in 45° position.

b) Ground CJ10-S.

c) Connect a DVM to the BJ21 test point and adjust R13 on BJ21 for zero drift of the DVM reading.

d) Move the DVM to the BJ28 test point and adjust R13 on BJ28 for zero drift of the DVM reading.

e) Remove ground from CJ10-S.

R - Integrator Final Adjust

a) Change AMPL to 0 - 1.5V.

b) Place LEAD switch in 0° position.

c) Adjust R24 on JB21 so that the 0° and 180° R readings are of equal amplitude.

d) Place LEAD switch in 90° position.

e) Adjust R24 on BJ28 so that the 90° readings are equal in both positions of the PHASE switch.

S - Summing Amplifier High Frequency Correction

a) Set the controls as follows:

AMPL	0-1.5V
FREQUENCY/Hz	9990 X 10°
INT	X1
LEAD	0°
DEMOD	OUT
MEASURE	RPT
MODE	R θ

b) Using a board extender, adjust C4 on BJ19 so that the "R" reading does not change as PHASE is switched between 0° and 180°.

c) Change LEAD to 90°.

d) Again using the board extender, adjust C4 on BJ26 so that the "R" reading does not change as PHASE is switched between 0° and 180°.

T - Input High Frequency and Phase Compensation

a) Set controls as follows:

AMPL	0 - 15V
INPUT RANGE	1.5V

b) Set OUTPUT for an "R" reading of approximately 1.500V

c) Alternately adjust C6 on CJ24 and C4 on CJ25 for a "θ" reading as close as possible to the selected lead angle and an "R" reading that does not vary more than 2 or 3 digits when the frequency is reduced to 9990 x 10^{-3}

NOTE: If a board extender is used, be sure to allow for the effects of the extender. It is particularily important when adjusting C6 because the accuracy of this adjustment affects all other input ranges.

d) Select .15 on the INPUT RANGE selector switch.

e) Select 0-1.5V on the AMPL switch.

f) Using the board extender, adjust C2 on CJ24 for minimum phase error on the readout.

g) Reduce OUTPUT until readings of about .0150 are achieved.

h) Select 90° on the LEAD switch.

i) Adjust C4 on BJ19 for minimum phase error in both positions of the PHASE switch.

j) Select 0° on the LEAD switch.

k) Adjust C4 on BJ26 for minimum phase error in both positions of the PHASE switch.

l) Select 15 on the INPUT RANGE selector switch.

m) Turn the OUTPUT control to maximum (CW).

n) Select 0-15V on AMPL switch.

o) Adjust C11 on CJ24 for minimum phase error on the readout.

p) Select 150 on the INPUT RANGE selector switch.

q) Choose a value for C15 on CJ24 that results in minimum phase error in the readout.

r) Unground the LO input jack and connect it to the OUTPUT jack.

s) Ground the HI input jack.

t) Select the 1.5 INPUT RANGE and adjust C6 on CJ28 for minimum phase error. Use sufficient input signal for a reading of about 1.500V.

u) Repeat steps d) through l) on CJ28.

5.3.5 - Carrier

A - Carrier Amplifier Adjustment

a) Ground BJ1-D.

b) Connect the DVM to TP1 on BJ1.

c) Adjust R9 on BJ1 for approximately zero volts.

d) Remove ground from BJ1-D.

B - Carrier Demodulator Offset Adjustment

a) Remove CJ25.

b) Ground CJ26-P

c) Connect a DVM to the test point on CJ26.

d) Ground CJ26-F and adjust R-26 on CJ26 for zero volts.

e) Remove the ground from CJ26-F and adjust R27 for zero volts.

f) Repeat d) and e) if necessary.

g) Remove the ground and replace CJ25.

C - Carrier Demodulator Threshold and Gain Adjustment

a) Set Controls as follows:

FUNCTION	AC Sine Wave
STOP	90°
BIAS	Center-Off Position
ampl	0-15v
OUTPUT	Clockwise
FREQUENCY/HZ	8000×10^{-2}
INT	X1
LEAD	0°
DEMOD	IN
MEASURE	RPT
RANGE	15v
DC REJECT	OFF
MODE	R θ

b) Connect the oscillator to the Carrier connectors.

c) Inject 800 cps at 10 v to 100 v rms from oscillator.

d) Connect an AC voltmeter to the OUTPUT jack and adjust LEVEL on the front panel until the voltmeter reads 10 VAC.

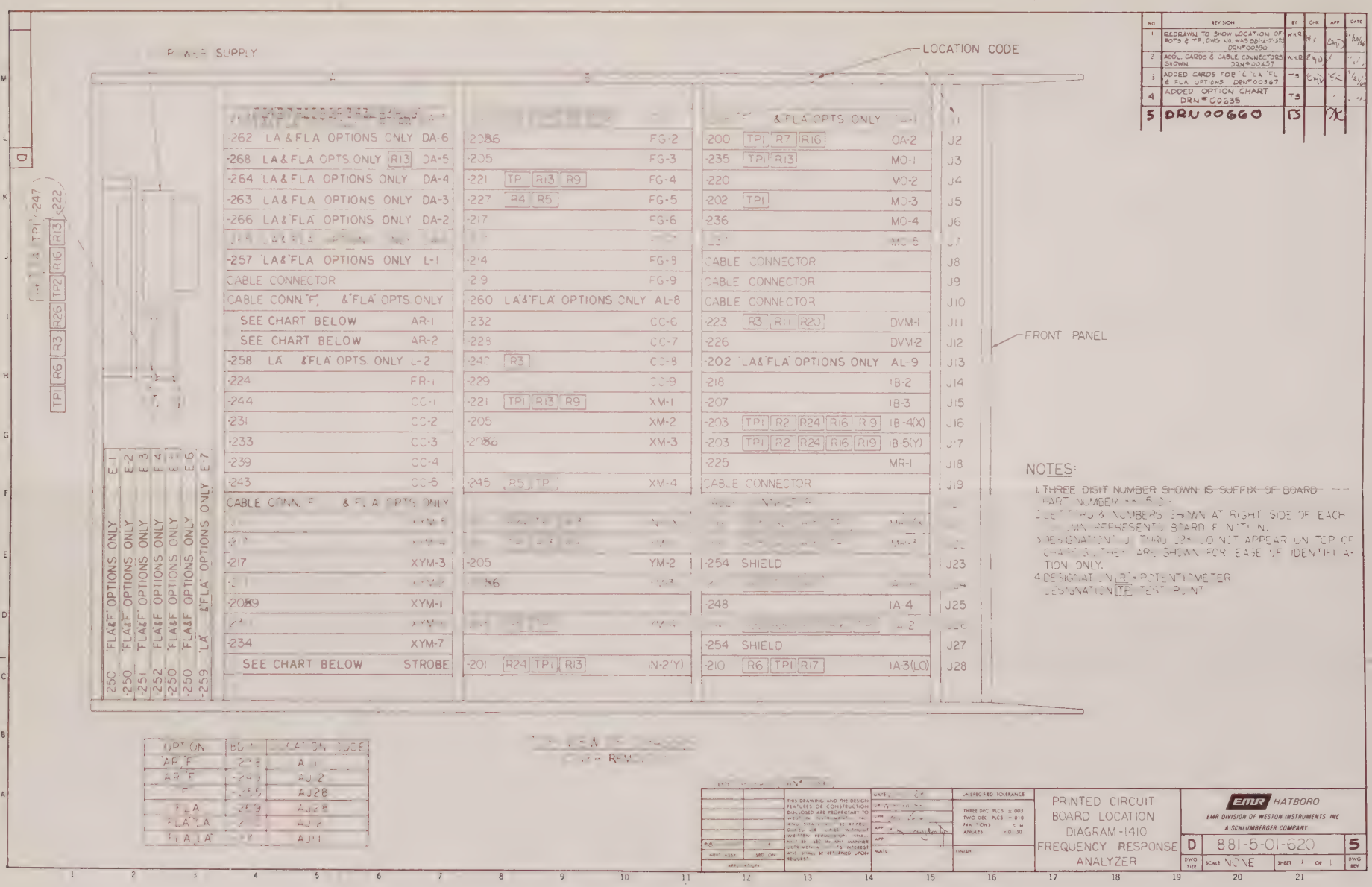
e) Connect the HI input jack to the OUTPUT jack and ground LO input.

f) Connect the scope probe to the test point on BJ26.

g) Adjust R22 on CJ26 for minimum offset between alternate half cycles on the scope presentation. (Scope sensitivity, 0.2v/cm).

h) Place STOP switch in center-off position.

i) Adjust R16 on CJ26 for an "R" reading of 14.14.


POWER SUPPLY
LOCATION CODE
FRONT PANEL
TP1 R6 R3 R26 TP2 R16 R13 -222 -247
-262 LA&FLA OPTIONS ONLY DA-6
-268 LA&FLA OPTS. ONLY R13 DA-5
-264 LA&FLA OPTIONS ONLY DA-4
-263 LA&FLA OPTIONS ONLY DA-3
-266 LA&FLA OPTIONS ONLY DA-2
-257 LA&FLA OPTIONS ONLY L-1
CABLE CONNECTOR
CABLE CONN. F & FLA OPTS. ONLY
SEE CHART BELOW AR-1
SEE CHART BELOW AR-2
-258 LA & FLA OPTS. ONLY L-2
-224 FR-1
-244 CC-1
-231 CC-2
-233 CC-3
-239 CC-4
-243 CC-5
CABLE CONN. F & FLA OPTS ONLY
-217 XYM-3
-2089 XYM-1
-234 XYM-7
SEE CHART BELOW STROBE
-2086 FG-2
-205 FG-3
-221 TP R13 R9 FG-4
-227 R4 R5 FG-5
-217 FG-6
FG-8
-214 FG-9
-219 FG-9
-260 LA&FLA OPTIONS ONLY AL-8
-232 CC-6
-228 CC-7
-240 R3 CC-8
-229 CC-9
-221 TP1 R13 R9 XM-1
-205 XM-2
-2086 XM-3
XM-4
-245 R5 TP XM-4
-205 YM-2
-2086 YM-4
-201 R24 TP1 R13 IN-2(Y)
-200 TP1 R7 R16 OA-2
-235 TP1 R13 MO-1
-220 MO-2
-202 TP1 MO-3
-236 MO-4
MO-5
CABLE CONNECTOR
CABLE CONNECTOR
CABLE CONNECTOR
-223 R3 R11 R20 DVM-1
-226 DVM-2
-202 LA&FLA OPTIONS ONLY AL-9
-218 IB-2
-207 IB-3
-203 TP1 R2 R24 R16 R19 IB-4(X)
-203 TP1 R2 R24 R16 R19 IB-5(Y)
-225 MR-1
CABLE CONNECTOR
-254 SHIELD
-248 IA-4
-254 SHIELD
-210 R6 TP1 R17 IA-3(LO)
J1 J2 J3 J4 J5 J6 J7 J8 J9 J10 J11 J12 J13 J14 J15 J16 J17 J18 J19 J23 J25 J27 J28
250 FLA&F OPTIONS ONLY E-1
-250 FLA&F OPTIONS ONLY E-2
-251 FLA&F OPTIONS ONLY E-3
-252 FLA&F OPTIONS ONLY E-4
-250 FLA&F OPTIONS ONLY E-5
-250 FLA&F OPTIONS ONLY E-6
-259 LA & FLA OPTIONS ONLY E-7
NOTES:
1. THREE DIGIT NUMBER SHOWN IS SUFFIX OF BOARD PART NUMBER 881-5-01-
2. DESIGNATORS & NUMBERS SHOWN AT RIGHT SIDE OF EACH J... MN REPRESENTS BOARD PIN N.
3. DESIGNATORS J THRU J25 DO NOT APPEAR ON TOP OF CHASSIS, THEY ARE SHOWN FOR EASE OF IDENTIFICATION ONLY.
4. DESIGNATOR R = POTENTIOMETER
DESIGNATOR TP = TEST POINT
OPTION | BD # | LOCATION CODE
AR-F | -247 | AJ1
AR-F | -247 | AJ2
F | -255 | AJ28
F LA | -259 | AJ28
FLA LA | -2 | AJ2
FLA LA | -2 | AJ1
NO | REVISION | BY | CHK | APP | DATE
1 | REDRAWN TO SHOW LOCATION OF POTS & TP, DWG NO. WAS 881-5-01-570 DRN#00390 | W.K.B. | | | 3/4/76
2 | ADDL CARDS & CABLE CONNECTORS SHOWN DRN#00457 | W.K.B. | | | 4/5/76
3 | ADDED CARDS FOR F, LA, FL & FLA OPTIONS DRN#00567 | T.S. | | | 3/23/76
4 | ADDED OPTION CHART DRN#00635 | T.S. | | | 4/1/76
5 | DRN 00660 | T.S. | | | 5/3/76
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UNSPECIFIED TOLERANCE
THREE DEC PLCS ± .005
TWO DEC PLCS ± .010
FRACTIONS ± 1/64
ANGLES ± 01'30
PRINTED CIRCUIT BOARD LOCATION DIAGRAM-1410 FREQUENCY RESPONSE ANALYZER
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
D
881-5-01-620
5
DWG SIZE
SCALE NONE
SHEET 1 OF 1
DWG REV

5.4 - TROUBLESHOOTING

5.4.1 - General

The troubleshooting approach described here is intended to help the user localize the fault to a board or a small group of boards. The goal can best be served by starting with a sequence that outlines the measurement process and relating the major logic and analog functions to the steps of the sequence. Greater detail can be found in the theory of operation (Section 4) if it is necessary.

5.4.2 - Operating Sequence

The following sequence outlines the steps involved in a single measurement.

1) The generator runs continually.

2) A measurement is initiated.

3) The correlator synchronizes to the generator.

4) The correlator measures and stores the rectangular components of the resultant.

5) Computation is automatically initiated.

6) The polarity of the component vector is sensed to determine the quadrant in which the resultant lies.

7) The coordinates are routed back through the multipliers to solve for θ.

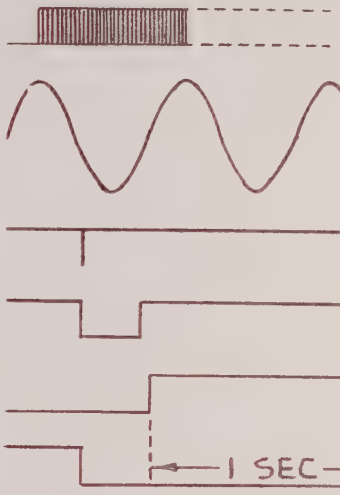
8) The coordinates are re-routed through the opposite multipliers to solve for R.

9) Measurement is complete.

5.4.3 - Timing Diagram

The timing diagram which follows relates to the major steps listed under Operating Sequence. Its purpose is to verify that the instrument is properly sequencing, or if not, to indicate at what step of the sequence a fault exists. This is particularly valuable in tracing faults that prevent MEAS COMPL from appearing on the front panel due to an incomplete sequence. Also, it is helpful to use the waveforms shown, in conjunction with a dual trace oscilloscope to examine the operation of some of the analog boards during a particular step of the Operating Sequence.

NAME	SEQUENCE	PIN LOCATION
DIVIDED CLOCK PULSE	(1)	CJ7-M
OUTPUT	(1)	FRT. PANEL
COMMAND CHAIN RESET	(2)	AJ15-D
SYNC. TIME COMPLETE	(3)	AJ16-P
INTEGRATE	(4)	AJ18-F
1 SECOND	(4)	AJ18-T
COMPUTE	(5)	CJ18-L
STATE 1	(6)	BJ11-D
STATE 2 & 3	(6)	BJ11-C
STATE 3	(6)	BJ11-E
STATE 4, 5, 6 & 7	(7), (8)	BJ11-S
STATE 5	(7)	BJ11-N
STATE 7	(8)	BJ11-P
STATE 8	(9)	BJ11-F
DETECT	(6), (7), (8)	CJ12-C



B

* DEPENDENT UPON QUADRANT IN WHICH θ LIES

881-6-01-001	1410
NEXT ASSY.	USED ON
APPLICATION	

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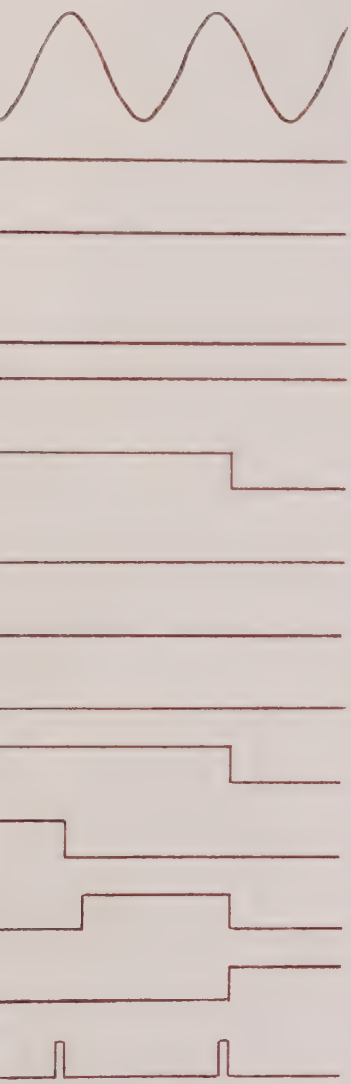
DATE	11-7-68
DR.	T. SMITH
CHK.	
APP.	
APP.	
MATL.	

UNSPECIFIED TOLERAN

THREE DEC. PLCS. ±.0
TWO DEC. PLCS. ±.0
FRACTIONS ±
ANGLES ±0°

FINISH

NO.	REVISION	BY	CHK.	APP.	DATE



FIRST RELEASE - DRN 00420

SIMPLIFIED
MING DIAGRAM

FIG. 5.2

EMR HATBORO

EMR DIVISION OF WESTON INSTRUMENTS, INC

A SCHLUMBERGER COMPANY

DWG. SIZE		DWG. REV.
B	881-3-01-073	0
SCALE NH	SECTION 5 PG. 26	

5.4.4 - Circuit Function

The following is a simplified theory of operation which references the Operating Sequence and Timing Diagram to the overall block diagram (Dwg. No. 881-5-01-602). References to the Operating Sequence and block diagram are shown in parenthesis throughout the explanation. If it is once established, from the logic signals, that the measurement sequence is being followed, examination of the related analog functions may be required.

The generator, to begin with, constructs a sine wave timed by clock pulses (DCP) from the master oscillator. These pulses are digitally processed to provide drive signals for the reference amplifier and the multiplier. The reference amplifier provides a precise square wave reference for the multiplier which in turn digitally steps the current input to the summing amplifier. The sine wave now present at the output of the summing amplifier is injected into the output amplifier which provides a low impedance drive to the output.

The sine wave input is accepted through one or both input amplifiers (Block No. 8) and is constantly present at the input to the multiplier routing board (Block No. 9). After Command Chain Reset (CCR) has prepared the instrument for the measurement just initiated (2) the synchronization circuit phase-locks the correlator to the generator (STC) and starts the measurement process coincident with a zero crossing of the generated sine wave (3). During integration (4) the signal, through multiplier routing, is connected to both the X channel (Blocks No. 5 and No. 6) and the Y Channel (Block No. 13 and No. 14). The synchronous demodulators act on the signal with a square wave of the same frequency as the generated sine wave. After being multiplied the signal appears at the output of the summing amplifier as a sine wave of twice the generated frequency with a DC component. The DC component is integrated over a period of not less than one second and ends when the integrate period contains an integral number of cycles. The results, which are stored in the integrators and scaled by the buffers, are rectangular components representing the desired answer.

Computation now begins (5). The first step is the determination of the polarity of the vector components (6) using the detector (Block No. 11). The polarity of the signal from the X buffer is determined using state 1 (6) and that of the Y buffer is determined during state 3. The results determine how the buffer signals are to be routed back through the multiplier routing board and into the multipliers for the determination of θ. (At this point the stored component vector can be measured by the simple method of grounding pin CJ10-S. This holds the instrument in state 5 (7) until the ground is removed.) To determine θ the routed signals are given the proper algebraic polarity by the demodulators, directed through the multiplier, summed in the

X ± Y amplifier and presented to the detector. The multipliers are then stepped until the detector indicates that the equation has been solved. The multipliers are stopped and held at that angle. The buffer signals are now routed back through the channel opposite to that used for θ, multiplied by the sine or cosine of θ and summed in the X ± Y amplifier. This sum is then compared with a ramp in the detector and the detector indicates when the value of R has been solved. The state generator sequences once more and the measurement is complete.

5.4.5 - Board Interchangeability

The following boards are electrically interchangeable and listed by location. Interchanging is useful in troubleshooting, but it is recommended that the boards be returned to their original location to prevent unnecessary recalibration of the instrument if possible.

AJ21	AJ24
AJ22	AJ23, BJ4, BJ7
AJ23	AJ22, BJ6, BJ7
AJ24	AJ21
BJ2	BJ17, BJ24
BJ3	BJ16, BJ23
BJ4	BJ15, BJ22
BJ6	AJ22, AJ23, BJ7
BJ7	AJ22, AJ23, BJ6
BJ15	BJ4, BJ22
BJ16	BJ3, BJ23
BJ17	BJ2, BJ24
BJ19	BJ26
BJ21	BJ28
BJ22	BJ4, BJ15

BJ23	BJ3, BJ16
BJ24	BJ2, BJ17
BJ26	BJ19
BJ28	BJ21
CJ16	CJ17
CJ17	CJ16
CJ21	CJ22
CJ22	CJ21
CJ24	CJ28
CJ28	CJ24

5.4.6 - Option F, Remote Readout

If the remote readout is not working properly, check the local readout to be sure the problem is in the remote section. If the remote readout is not the same as the local readout then refer to block diagram number 881-6-01-623 and trace the signal from its origin to the output connector (J105). This can be done in two ways; by logically tracing the signal through each component or by comparing the logic levels of the malfunctioning line with those of a line that is functioning properly.

5.4.7 - Option F, Remote Programming

If all functions of the unit can not be programmed, check the program with the procedure stated in Sections 3, 6 and 2.9. If the unit is programmed properly and still does not operate, put the remote manual switch in the manual position and program the same functions from the front panel. If the instrument works properly in manual operation then the problem is in the remote section. Refer to block diagram number 881-6-01-622 and trace the command from the input connector (J106) to its destination in the P/C card frame assembly. This can be done in two ways; by logically tracing the signal through each component or by comparing the logic levels of the malfunctioning line with those of a line that is functioning properly.

To determine the voltage level that a command should be at its ultimate destination in the P/C card frame assembly, make the same command from the front panel in manual operation. At this point in the circuit the command should be at the same level regardless of where the command comes from.

5.4.8 - Options AR and F, Auto Ranging

If the instrument does not change ranges properly check Section 3.8 to see if its limits are being exceeded. If the instrument is being operated within its range and still does not work properly then refer to wiring diagram number 881-5-01-621.

6 - CIRCUIT DIAGRAMS

6.1 - Printed Circuit Board Schematic Diagrams - Standard 1410

For Units containing options, check the option schematic section for schematics that supersede standard schematics.

Schematic No.	Function	Card Slot	Title
881-5-01-100	OA-2	CJ2	Output Amplifier
101	IN-1, IN-2	BJ21, BJ28	Integrator
102	MO3	CJ5	Master Oscillator, Coincidence Counter
103	1B-4, 1B-5	CJ16, 17	Integrator Buffer Weighting
105	FG-3, XM-2 YM-2	BJ3, BJ16 BJ23	10° Weighting
106	FG-2, XM-3, YM-3	BJ2, BJ17, BJ24	10° Steps
107	1B-3	CJ15	Integrator Buffer Drive
109	XYM-1	AJ25	1° Generator X & Y Mult.
110	1A-1, 1A-3	CJ24, CJ28	Input Amplifier
111	XYM-2 XYM-5	AJ21, AJ24	Drive Logic, 1° & .1° Gen. X & Y Mult.
114	FG-8	BJ8	1° Counter, 10° Logic for Function Generator
115	Display	Sub Panel	Display
116	MR-2, MR-3	CJ21. 22	Synchronous Demodulator
117	FG-6, FG-7, XYM-3, XYM-4	AJ22, 23, BJ6, 7	Shift Register
118	1B2	CJ14	Integrator Buffer
119	FG-9	BJ9	90° & 180° FF, Function Gen.
120	MO-2	CJ4	Divided Clock Pulse
121	FG-4, XYM-1, YM-1	BJ4, BJ15, BJ22	1° Step Generator

Schematic No.	Function	Card Slot	Title
881-5-01-122	±20v reg.	P. S. Top	±20 v regulator
123	DVM-1	CJ11	Ramp & Y ± Y Generator
124	FR-1	AJ-14	Primary Frequency Generator
125	MR-1	CJ18	Multiplier Routing
126	DVM-2	CJ12	Error Detect
127	FG-5	BJ5	Reference Amplifier
128	CC-7	BJ12	X & Y Pol FF, R & θ Reg. Gating
129	CC-9	BJ14	Detect Switching
130	XYM-6	AJ26	1° Counter, 90° FF (Corr.)
131	CC2	AJ16	Synchronization
132	CC-6	BJ11	State Counter
133	CC-3	AJ17	Sampling
134	XYM-7	AJ27	180° & 270° FF (Corr)
135	MO-1	CJ3	Master Oscillator Control
136	MO-4	CJ6	Master Oscillator Capacitor Switching
137	MO-5	CJ7	Variable Frequency Pulse Generator
139	CC-4	AJ18	Integrator Com'd Gen.
140	CC-8	BJ13	DVM Switching
141	1A-2	CJ26	Carrier Demodulator
142	FG-1	BJ1	Summation & Carrier Amp.
143	CC-5	AJ19	X10 Int., Switching logic for integrator
144	CC-1	AJ15	Starting Logic
145	XM-4, YM-4	BJ19, BJ26	Summation Amplifier
147	+5V Reg	P. S. Bottom	+5V regulator
148	1A-4	CJ25	Mixer Amplifier

6.2 - Block and Wiring Diagrams - Standard 1410

For units containing options, check the option schematic section for schematics that supersede standard schematics.

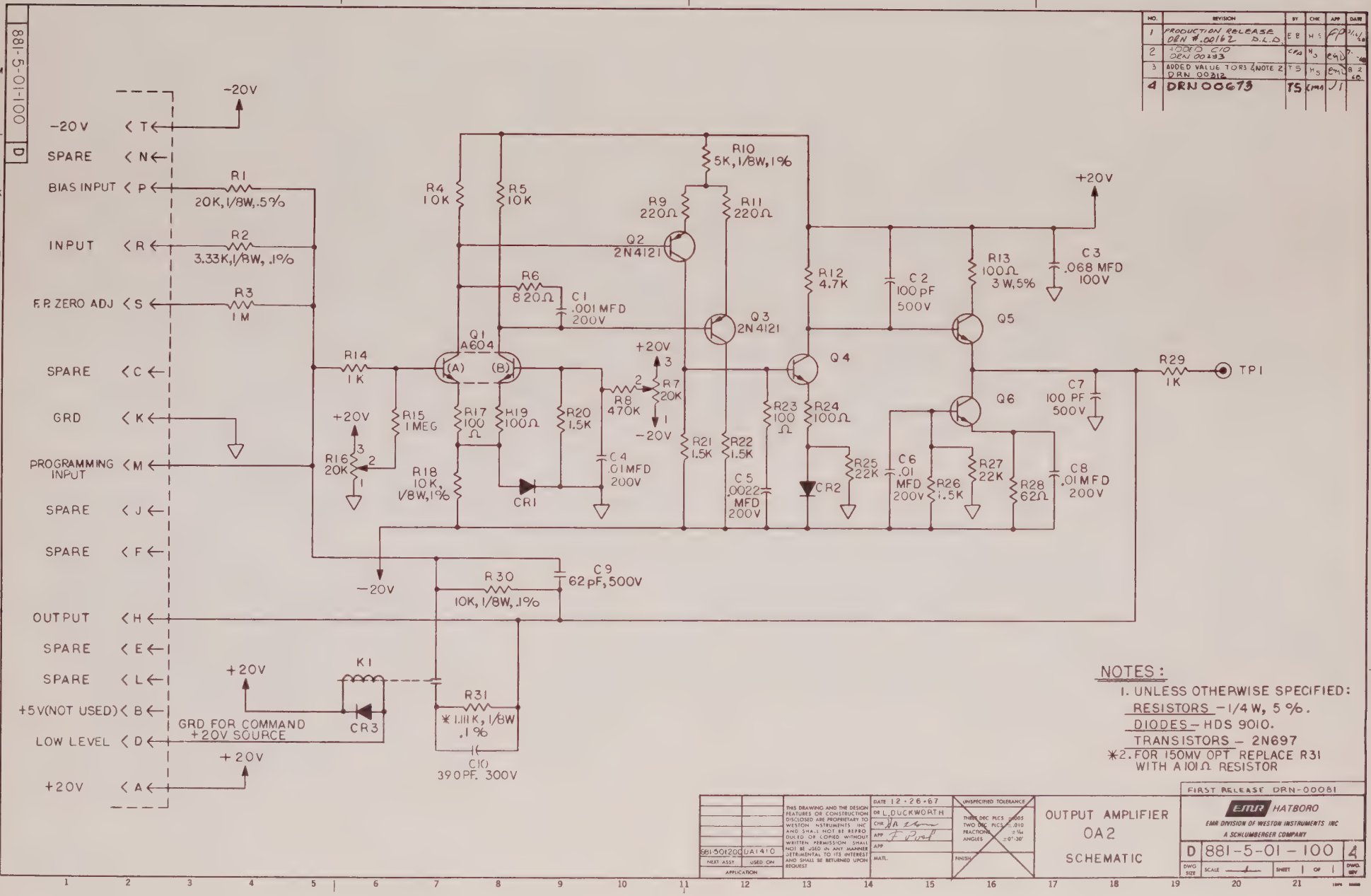
Schematic No.	Title
881-5-01-600	Sub Panel Wiring Diagram (Does Not Apply to "F" , or "P" Opt).
602	Overall Block Diagram
603	Power Supply Wiring Diagram
604	Y Multiplier Analog Circuitry
605	X Multiplier Analog Circuitry
606	Integrators & Int. Buffers
607	Master Oscillator
608	Function Generator
610	Command Chain Logic
611	Input Amplifiers
881-6-01-612	Driving & Logic Circuitry for X & Y Mult & X & Y Demod
613	State Counter & Command Generator

6.3 - Printed Circuit Board Schematic Diagrams for F, and AR Options

Schematic No.	Option	Function	Card Slot	Title
881-5-01-108	F	OA-1	CJ1	Remote Amplitude Programming
138	AR, F	AR-1	AJ11	Auto-Ranging
149	AR, F	AR-2	AJ12	Auto-Decimal Drivers
150	P, F	In/Out Buffer	E1, E2, E5, E6	In/Out Interface Remote Control
151	F	Lamp/Relay Driver	E3	Gated Relay/ Lamp Driver
152	F	Logic Levels	E4	Manual Command Buffers
155	F	Strobe	AJ28	Output Strobe

6.4 - Block and Wiring Diagrams For F, P, and AR Options

881-5-01-618	F	Sub Panel Wiring	Use in lieu of 881-5-01	600
3 616	F	Rear Panel Wiring		
6 623	F	Block Diagram of Read-out Circuitry		
6 622	F	Block Diagram of Remote Programming Circuitry		
5 621	AR, F	Wiring Diagram of Auto-Ranging		



NO.	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN #.00162 D.L.D.	E B	M S	[illegible]	[illegible]
2	ADDED C10 DRN 00233	C P D	M S	[illegible]	[illegible]
3	ADDED VALUE TO R3 (NOTE 2) DRN 00212	T S	M S	[illegible]	[illegible]
4	DRN 00673	T S	[illegible]	J I	

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
RESISTORS – 1/4 W, 5 %.
DIODES – HDS 9010.
TRANSISTORS – 2N697
*2. FOR 150MV OPT REPLACE R31 WITH A 101Ω RESISTOR

FIRST RELEASE DRN-00081

DATE 12-26-67	UNSPECIFIED TOLERANCE	OUTPUT AMPLIFIER	EMR HATBORO
DR L. DUCKWORTH	THREE DEC PLCS ±.0005 TWO DEC PLCS ±.010 FRACTIONS ±1/64 ANGLES ±0°-30'	0A2	EMR DIVISION OF WESTON INSTRUMENTS INC A SCHLUMBERGER COMPANY
CHK [illegible]		SCHEMATIC	D 881-5-01-100 4
APP F. Rich	FINISH		DWG SIZE SCALE — SHEET 1 OF 1 DWG REV
APP			
MATL.			

881501200 UA1410
NEXT ASSY. USED ON
APPLICATION

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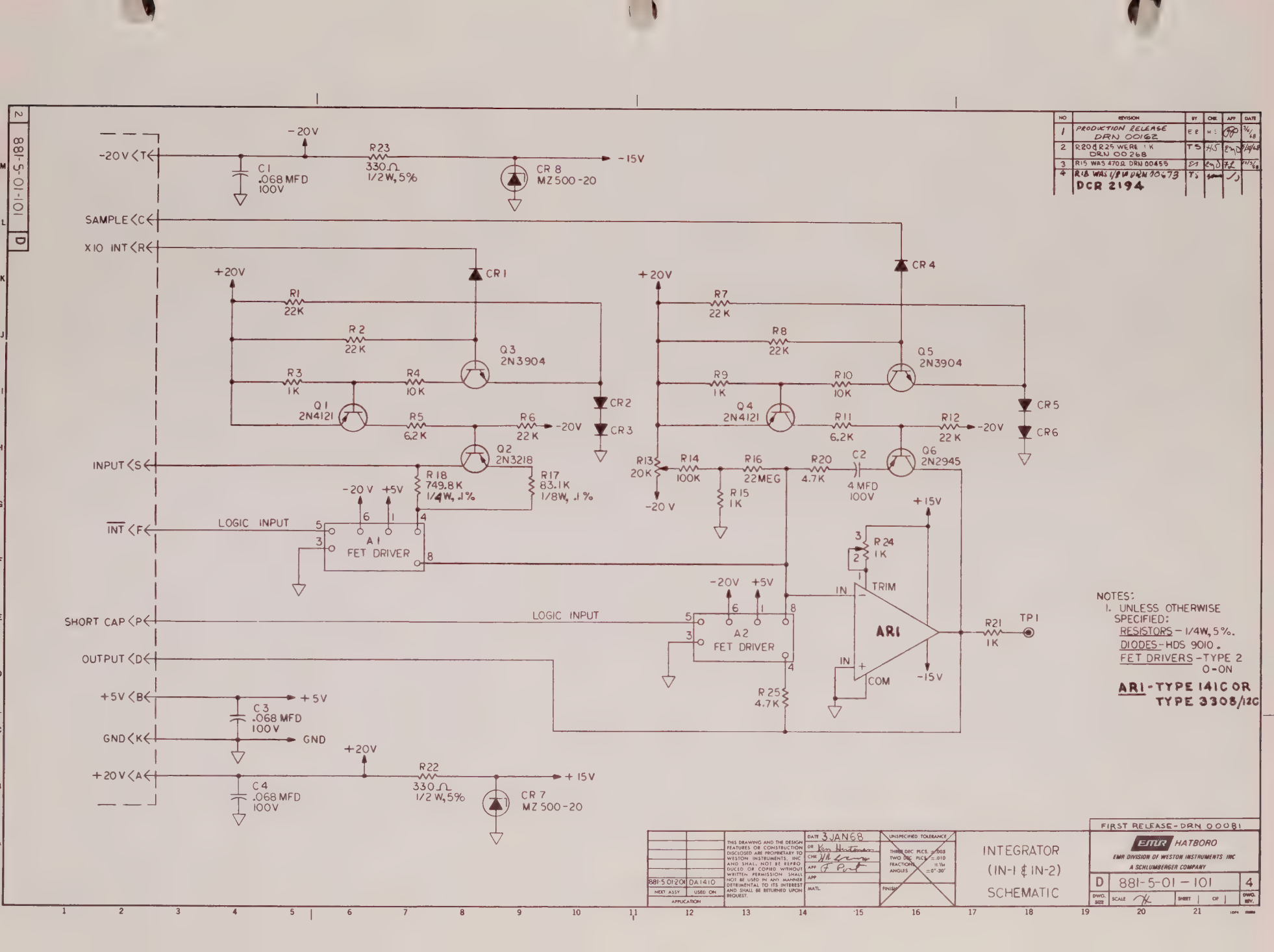

NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN 00162	E E	M L		3/1/68
2	R20 & R25 WERE 1K DRN 00268	T S			5/14/68
3	R15 WAS 470Ω DRN 00455				11/5/68
4	R18 WAS 1/8W DRN 00673 DCR 2194	T S			

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
RESISTORS – 1/4W, 5%.
DIODES – HDS 9010.
FET DRIVERS – TYPE 2 O-ON

ARI – TYPE 141C OR TYPE 3308/12C

FIRST RELEASE – DRN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

INTEGRATOR (IN-1 & IN-2) SCHEMATIC

881-5-01-101 D 4

881-5-01-201 DA1410

DATE 3 JAN 68
DR Ken Hartman
CHK
APP
APP
MATL

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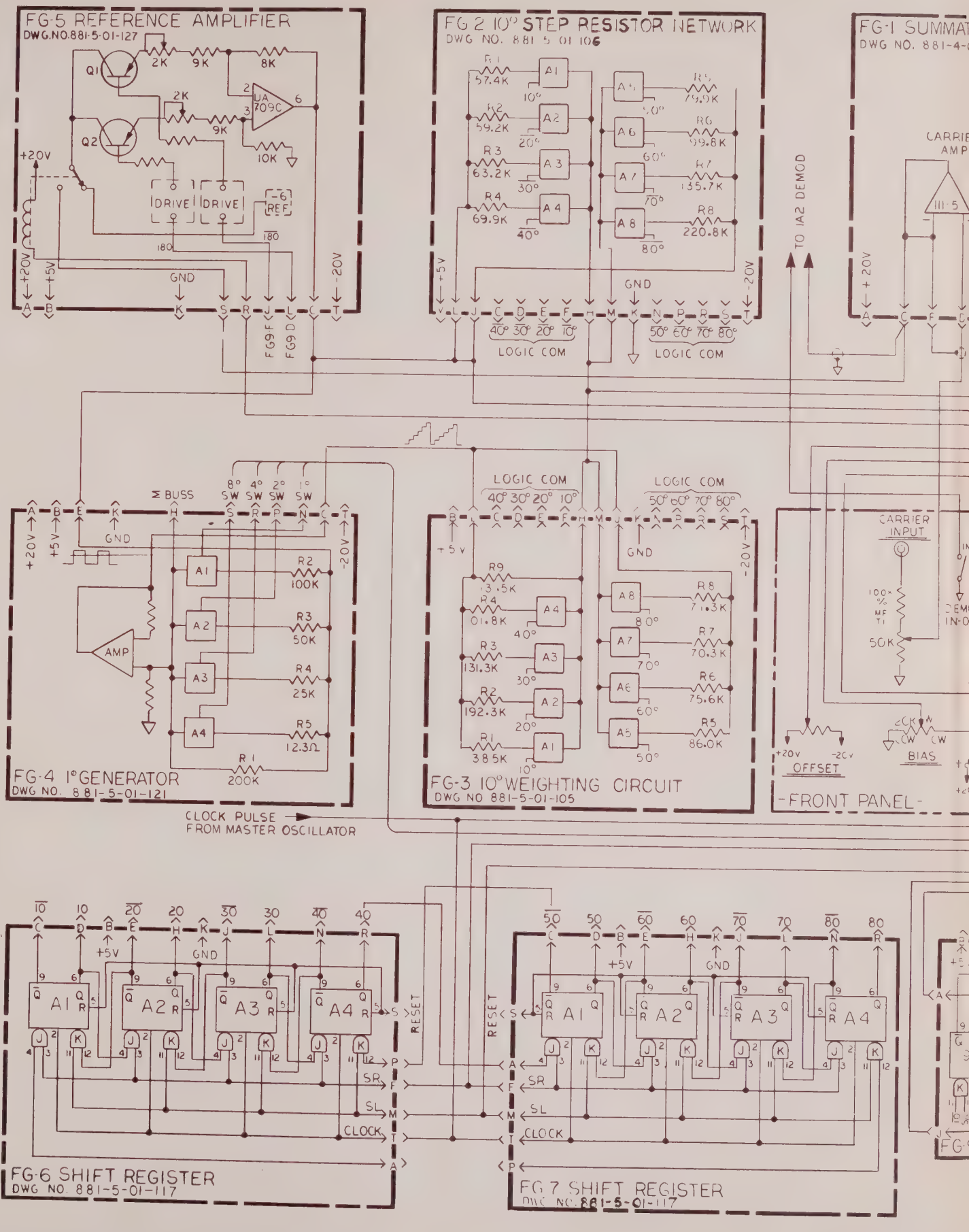
UNSPECIFIED TOLERANCE
THREE DEC PLCS. ±.005
TWO DEC PLCS. ±.010
FRACTIONS ±1/64
ANGLES ±0°-30'

FINISH

SHEET 1 OF 1


FG-5 REFERENCE AMPLIFIER
DWG.NO.881-5-01-127
Q1
Q2
2K
9K
8K
10K
UA 709C
+20V
DRIVE
DRIVE
REF
180
GND
-20V
FG9 F
FG9 D
FG 2 10° STEP RESISTOR NETWORK
DWG NO. 881 5 01 106
R1 57.4K
R2 59.2K
R3 63.2K
R4 69.9K
R5 79.9K
R6 99.8K
R7 135.7K
R8 220.8K
A1
A2
A3
A4
A5
A6
A7
A8
10°
20°
30°
40°
50°
60°
70°
80°
LOGIC COM
TO IA2 DEMOD
FG-1 SUMMAT
DWG NO. 881-4-
CARRIE
AMP
III-5
+ 20V
Σ BUSS
8° SW
4° SW
2° SW
1° SW
AMP
R1 200K
R2 100K
R3 50K
R4 25K
R5 12.3Ω
FG-4 1°GENERATOR
DWG NO. 881-5-01-121
R9 13.5K
R4 01.8K
R3 131.3K
R2 192.3K
R1 385K
R8 71.3K
R7 70.3K
R6 75.6K
R5 86.0K
FG-3 10°WEIGHTING CIRCUIT
DWG NO 881-5-01-105
CARRIER INPUT
100K % MF TI
50K
OFFSET
BIAS
-FRONT PANEL-
CLOCK PULSE FROM MASTER OSCILLATOR
A1
A2
A3
A4
SR
SL
CLOCK
RESET
FG-6 SHIFT REGISTER
DWG NO. 881-5-01-117
FG-7 SHIFT REGISTER
DWG NO. 881-5-01-117
FIRST RELEASE-D

NO	REVISION	BY	APP	DATE
1	DRN 00641	TS	JRS	9/24/82

ON & CARRIER AMP
-142

SUMMATION AMP

18-A

0A2 OUTPUT AMPLIFIER
DWG NO 881-4-01-100

R31 1110Ω

R30, 0K

+20V

OUTPUT

GND

1.5V COMMAND

R3 OFFSET

R4 BIAS

R5 3.33K INPUT

-20V

AUTO MAN

IV 8V 4V 2V 1V

GND

R1 500K R2 6.25K R3 12.50K R4 25.0K R5 50.0K R6 100K R7 200K R8 400K R9 800K

K1 K2 K3 K4 K5 K6 K7 K8 K9

10V 8V 4V 2V 1V .8V .4V .2V .1V

0A1 REMOTE AMP PROG
DWG NO 881-4-01-108

0V 8V 4V 2V 1V .8V .4V .2V .1V AUTO MAN

REMOTE COMMAND CABLE

NOTE: GROUND LINE FOR COMMAND
EXAMPLE - GROUND "8V" FOR OUTPUT
SIGNAL OF ±8VOLTS PEAK

FUNCTION SELECTOR SWITCH

PHASE SW

CLOCK

STOP 0

1°SWK

2°SWK

4°SWK

1°

50°

S/R

+5V

8°SWK

S/LK

90°

8°

4°

180°

10

90°

GND

180FF A2

90° & 180°FF DWG NO. 881-5-01-119

SN7490

R(0) R(9)

A1 A7

FG-8 1° COUNTER & 10° LOGIC
DWG NO 881-5-01-114

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PROJECT NO.	
DATE:	5 JULY 82
DRAWN:	J N B
CHECKED:	
APPROVED:	
SCALE:	

UNSPECIFIED TOLERANCE
TWO DEC. PLACES ± .010
THREE DEC. PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0° 30'
MATERIAL:
PROTECTIVE FINISH:
QUANT. PER ASS'Y:

BLOCK & INTERCONNECTION DIAGRAM FUNCTION GENERATOR-DA1410

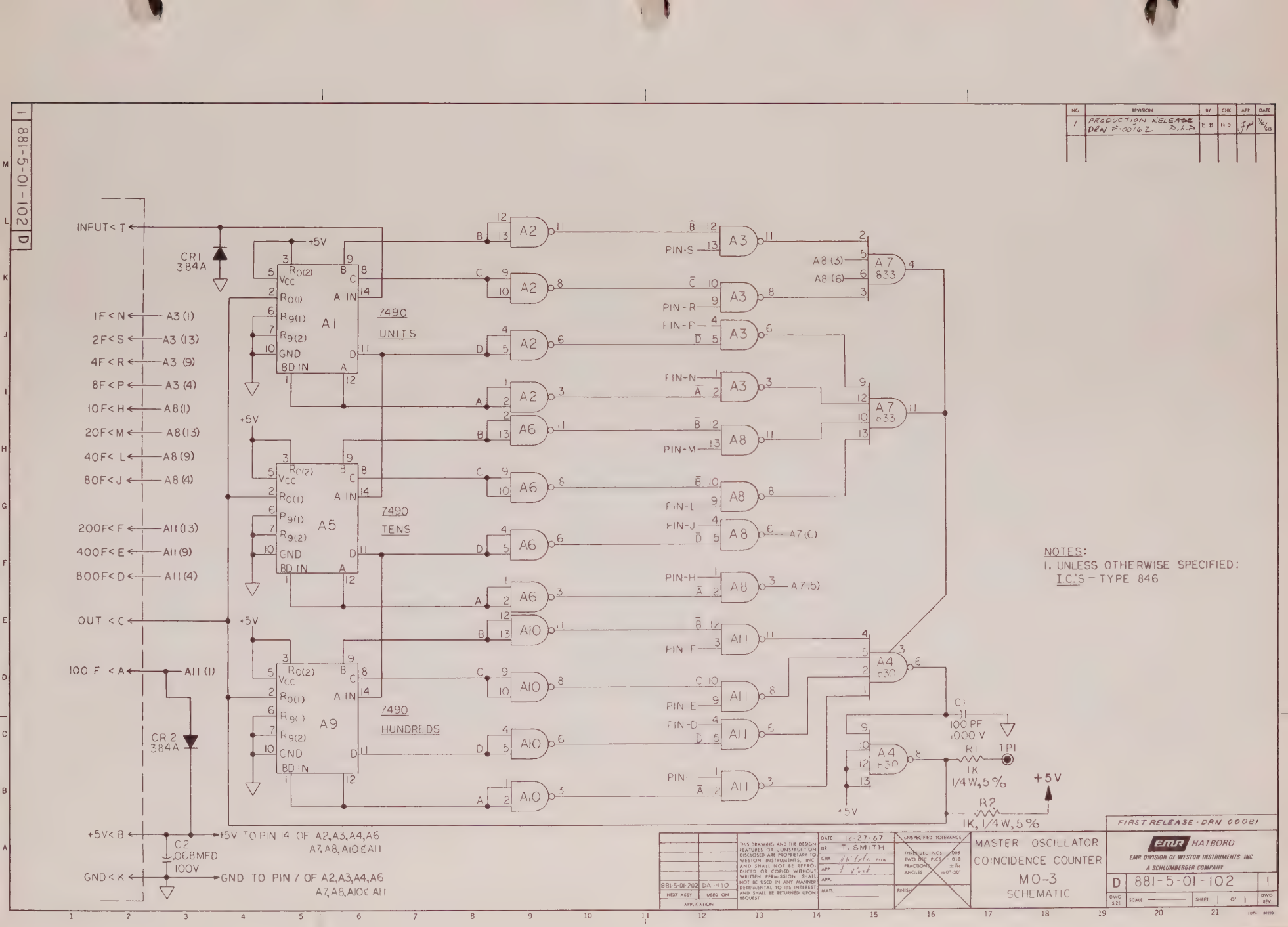
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC

DRAWING NUMBER	REV.
881-5-01-608	1

1410

00312

3 2 1



NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN #-00162 R.A.R.	E B	H S	JP	3/4/68

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   I.C.'S - TYPE 846

DATE	12-27-67	UNSPECIFIED TOLERANCE	MASTER OSCILLATOR COINCIDENCE COUNTER MO-3 SCHEMATIC
DR	T. SMITH	THREE DEC PLCS ±.005 TWO DEC PLCS ±.010 FRACTIONS ±1/64 ANGLES ±0°-30'	
CHK			
APP			
APP.			
MATL		FINISH	

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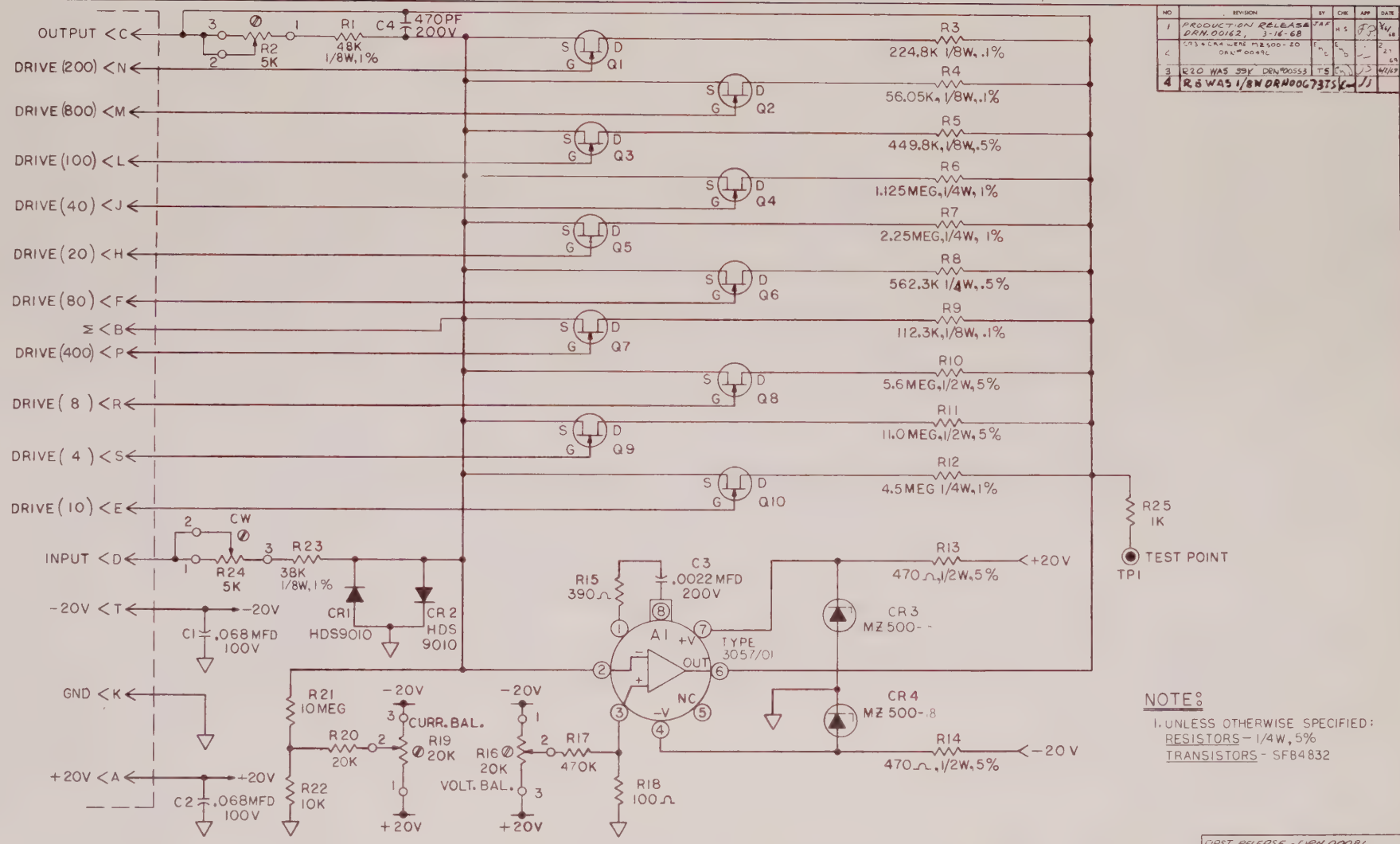
881-5-01-202 DA 410
NEXT ASSY | USED ON
APPLICATION

FIRST RELEASE - DRN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D | 881-5-01-102 | 1
DWG SIZE | SCALE | SHEET 1 OF 1 | DWG REV.

881-5-01-102 D



NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN. 00162, 3-16-68	JAF	HS	FP	4/4/68
2	CR3 & CR4 WERE MZ500-20 DRN 00494C	EC	CD	—	2-27-69
3	R20 WAS 39K DRN 00553	TS	CD	JJ	4/4/69
4	R8 WAS 1/8W DRN 00673 TS			JJ	

NOTES

1. UNLESS OTHERWISE SPECIFIED:
   RESISTORS – 1/4W, 5%
   TRANSISTORS – SF84832

FIRST RELEASE - DRN 00081

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DATE 12-28-67
DR KEN CONTE
CHK
APP
APP
MATL

UNSPECIFIED TOLERANCE
THREE DEC PLCS ±.005
TWO DEC PLCS ±.010
FRACTIONS ±1/64
ANGLES ±0°30'
FINISH

881-5-01-103 D
NEXT ASSY | USED ON
APPLICATION

INTEGRATOR BUFFER WEIGHTING CIRCUIT IB-4 & IB-5 SCHEMATIC

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D 881-5-01-103 4

DWG SIZE | SCALE | SHEET 1 OF 1 | DWG REV

NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DAN #-00162	E.B	H.S	[illegible]	3/4/68

881-5-01-105 D

+5V B → 1
GND K → 3
20V T → 6
} A1 THRU A8

DTL SIG IN 40° C
DTL SIG IN 30° D
DTL SIG IN 20° E
DTL SIG IN 10° F
Σ BUS H

A1 (5 6 7 8 / 1 2 3 4) — R1 385K 1/8W, 0.5%
A2 (5 6 7 8 / 1 2 3 4) — R2 192.3 1/8W, 0.5%
A3 (5 6 7 8 / 1 2 3 4) — R3 131.3K 1/8W, 0.5%
A4 (5 6 7 8 / 1 2 3 4) — R4 101.8K
R9 131.5K 1/8W, 1%

REF L
REF J

R5 86K — A5 (4 3 2 1 / 8 7 6 5)
R6 75.6K — A6 (4 3 2 1 / 8 7 6 5)
R7 70.3K — A7 (4 3 2 1 / 8 7 6 5)
R8 7.3K — A8 (4 3 2 1 / 8 7 6 5)

Σ BUS M
DTL SIG IN 50° N
DTL SIG IN 60° P
DTL SIG IN 70° R
DTL SIG IN 80° S

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
RESISTORS — 1/8W, 0.25%
MODULES — A1 THRU A8 - FET SWITCHING MODEL NO. 1

FIRST RELEASE - DAN 00081

THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION, SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST

DATE 1·4·67
DR T. SMITH
CHK [illegible]
APP. [illegible]
APP
MATL.
FINISH
UNSPECIFIED TOLERANCE: THREE DEC PLCS ±.005; TWO DEC PLCS ±.010; FRACTIONS ±1/64; ANGLES ±0°30'

10° WEIGHTING CIRCUIT FUNCTION GENERATOR AND CORRELATOR FG3, YM2 & XM2 SCHEMATIC

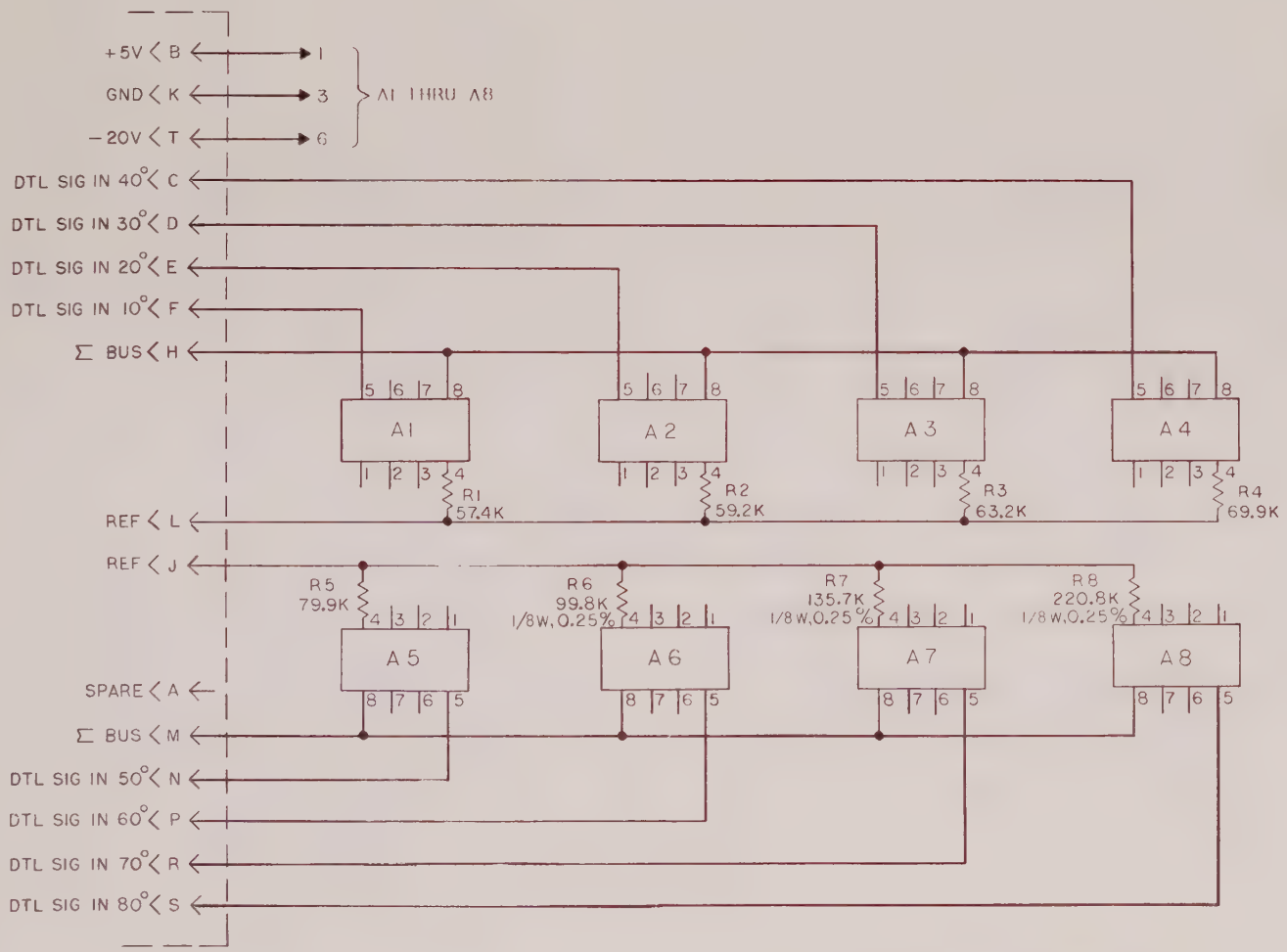
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

D | 881-5-01-105 | 1

DWG SIZE | SCALE | SHEET 1 OF 1 | DWG REV

881-5-01-105 DA1410
NEXT ASSY USED ON
APPLICATION

NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN #00162 S.S.	E.E.	W.S.	FP	3/1/68



NOTE:

1-UNLESS OTHERWISE SPECIFIED.
RESISTORS — 1/8W 0.1%.
MODULES — A1 THRU A8 - FET SWITCHING MODEL NO. 1

FIRST RELEASE - DRN 00081

10° STEP RESISTOR NETWORK FUNCTION GEN. E CORRELATOR IG 2, XM 3, YM 3 SCHEMATIC	EMR HATBORO, EMR DIVISION OF WESTON INSTRUMENTS, INC, A SCHLUMBERGER COMPANY	D	8215-01-106	1
		DWG SIZE	SCALE 1/1	SHEET 1 OF 1

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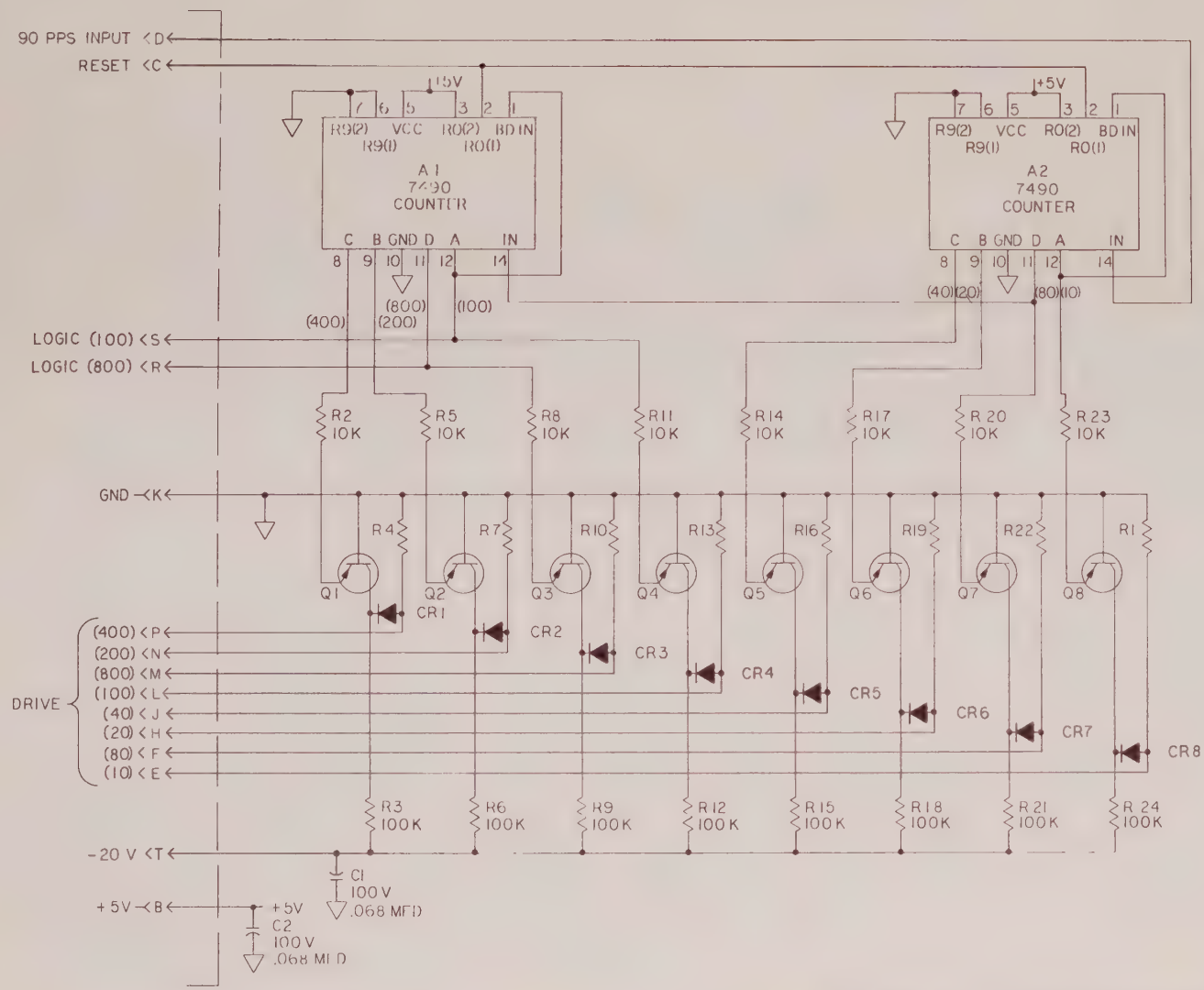
DATE 12-21-67
DR MINICHIELLO
CHK
APP
APP
MATL
FINISH
UNSPECIFIED TOLERANCE
THREE DEC PLCS ±.005
TWO DEC PLCS ±.010
FRACTIONS ±1/64
ANGLES ± 30'
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING



NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN # 00162 CPA	E B	H S	GP	9/14/67

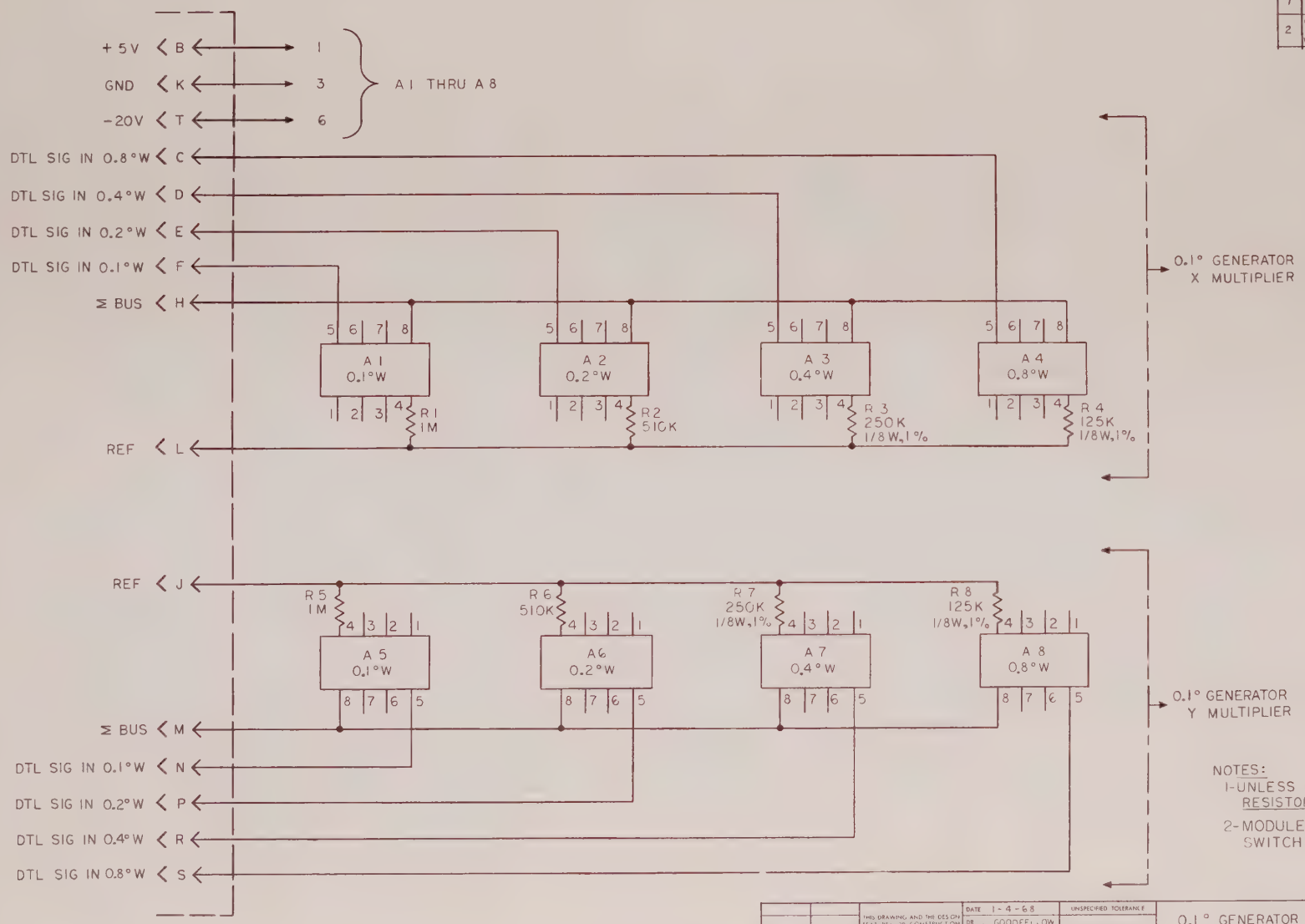
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTORS - 1/4W, 5%
   DIODES - HDS9010
   TRANSISTORS - 2N4121
2. RESISTORS R1, R4, R7, R10, R13, R16, R19, & R22 ARE 390K.

FIRST RELEASE - DRN 00081

		THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION, SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST	DATE 20 SEPT. 67 DR. G. J. Fitzgerald CHK. M. S. Grimm APP. C. Kent APP MATL	UNSPECIFIED TOLERANCE THREE DEC PLCS. ±.005 TWO DEC PLCS. ±.010 FRACTIONS ±1/64 ANGLES ±0°-30'	INTEGRATOR BUFFER DRIVE CIRCUIT (10-800 WT) IB3 SCHEMATIC	EMR HATBORO EMR DIVISION OF WESTON INSTRUMENTS, INC A SCHLUMBERGER COMPANY D 881-5-01-107 1 DWG SIZE SCALE NONE SHEET 1 OF 1 DWG REV.

881-5-01-107 D



NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN #.00162 A.L.D.	E B	M S	[illegible]	3/14/68
2	R1 R5 WERE 470K; R2, R6 WERE 240K; R3, R7 WERE 125K, R4, R8 WERE 62.2K. DRN NO. 00283	E B	M S	—	6/28/68

NOTES:
1-UNLESS OTHERWISE SPECIFIED
RESISTORS - 1/2 W, 5 %
2-MODULES A1 THRU A8 — FET SWITCHING MODEL NO.1.

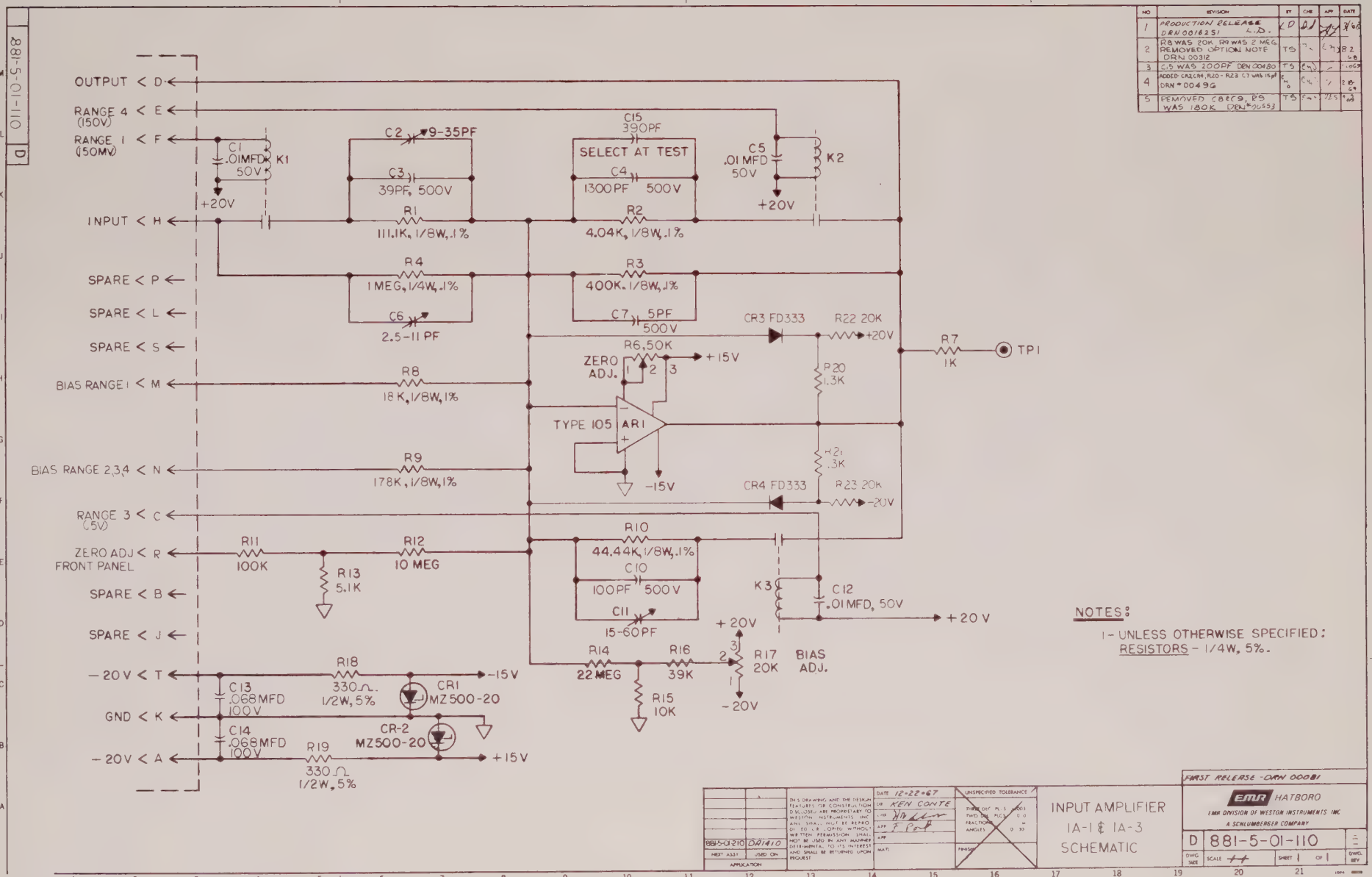
FIRST RELEASE-DRN 00081

881-5-01-204-DA141C		THIS DRAWING AND THE DESIGN FEATURES IT CONSTRUCTION IS SUGGESTED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC. AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION. SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST	DATE 1-4-68	UNSPECIFIED TOLERANCE	0.1° GENERATOR X & Y MULTIPLIER XYM-1 SCHEMATIC
NEXT ASSY	USED ON		DR GOODFELLOW	THREE DEC PLCS .005 TWO DEC PLCS .010 FRACTIONS 1/16 ANGLES ±0° 30'	
APPLICATION			CHK		
			APP		
			APP		
			MATL	FINISH	

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D	881-5-01-109	2
DWG SIZE	SCALE NONE	SHEET 1 OF 1	DWG REV

881-5-01-109 D 2



NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN 00182SI K.D.	KD	DJ		8/66
2	R8 WAS 20K, R9 WAS 2 MEG. REMOVED OPTION NOTE DRN 00312	TS			8 2 68
3	C5 WAS 200PF DRN 00480	TS			10-69
4	ADDED C21, C19, R20 - R23 C7 WAS 15pF DRN # 00496				2 25 69
5	REMOVED CR1, CR2, R5 WAS 180K DRN #00553	TS			4-8-69

NOTES:

1 - UNLESS OTHERWISE SPECIFIED:
RESISTORS - 1/4W, 5%.

881-5-01-210	DA1410				
NEXT ASSY	USED ON				
APPLICATION					

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DATE 12-22-67
DR KEN CONTE
CH
APP
APP
MAT'L

UNSPECIFIED TOLERANCE
THREE DEC PLS ±.005
TWO DEC PLCS ±.01
FRACTIONS ±
ANGLES ±0 30'
FINISH

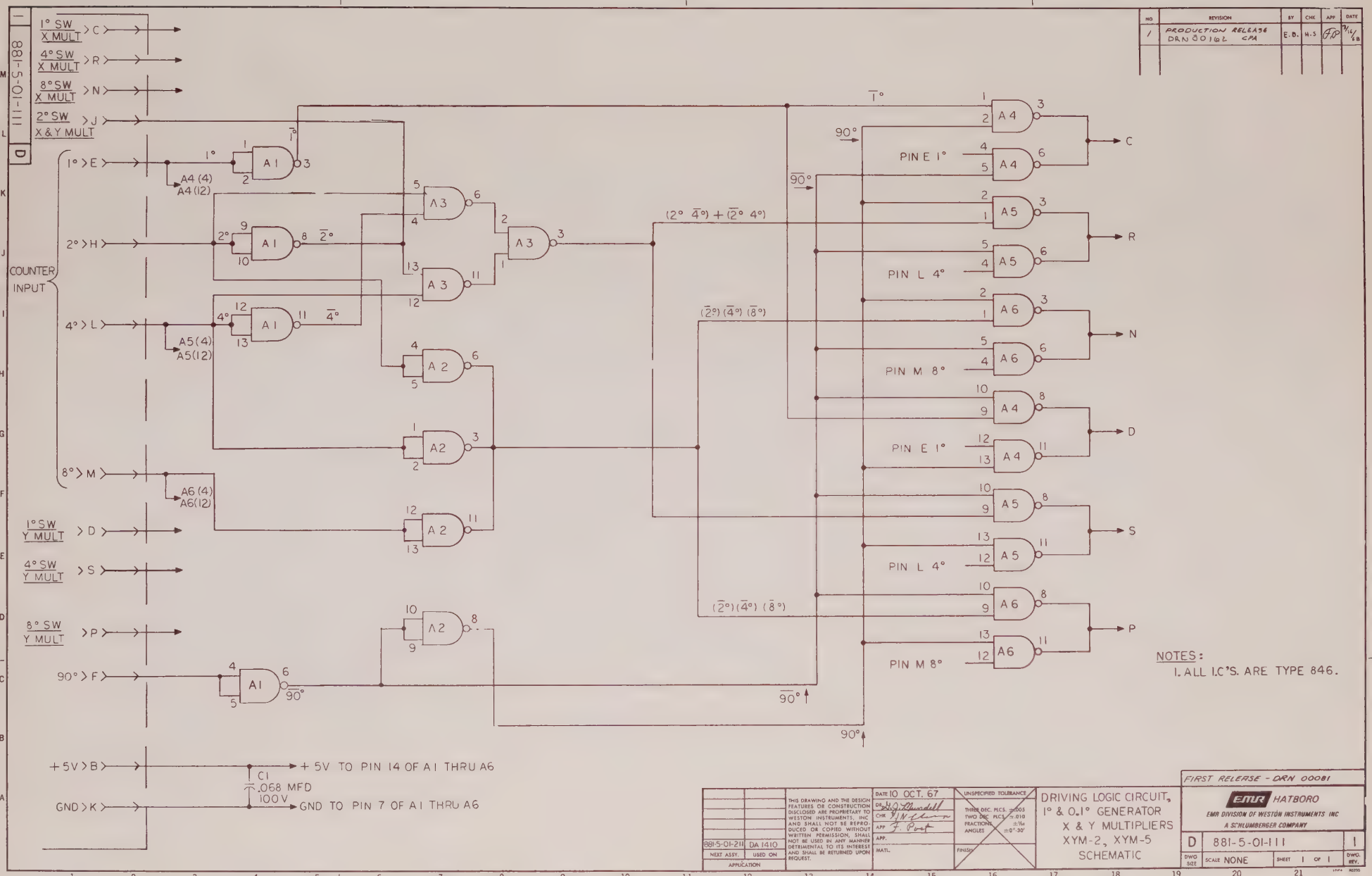
INPUT AMPLIFIER
1A-1 & 1A-3
SCHEMATIC

FIRST RELEASE - DRN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D | 881-5-01-110

DWG SIZE | SCALE 1/1 | SHEET 1 OF 1 | DWG. REV.



NOTES:
1. ALL I.C'S. ARE TYPE 846.

NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN 00182 CM	E.B.	H.S	GP	9/4/68

881-5-01-211	DA 1410		
NEXT ASSY.	USED ON		
APPLICATION			

THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION, SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST.

DATE 10 OCT. 67
DR H.J. Thrasdell
CHK H.W. Lemmon
APP F. Post
APP.
MATL.

UNSPECIFIED TOLERANCE
THREE DEC. PLCS. ±.005
TWO DEC. PLCS. ±.010
FRACTIONS ±1/64
ANGLES ±0°-30'
FINISH

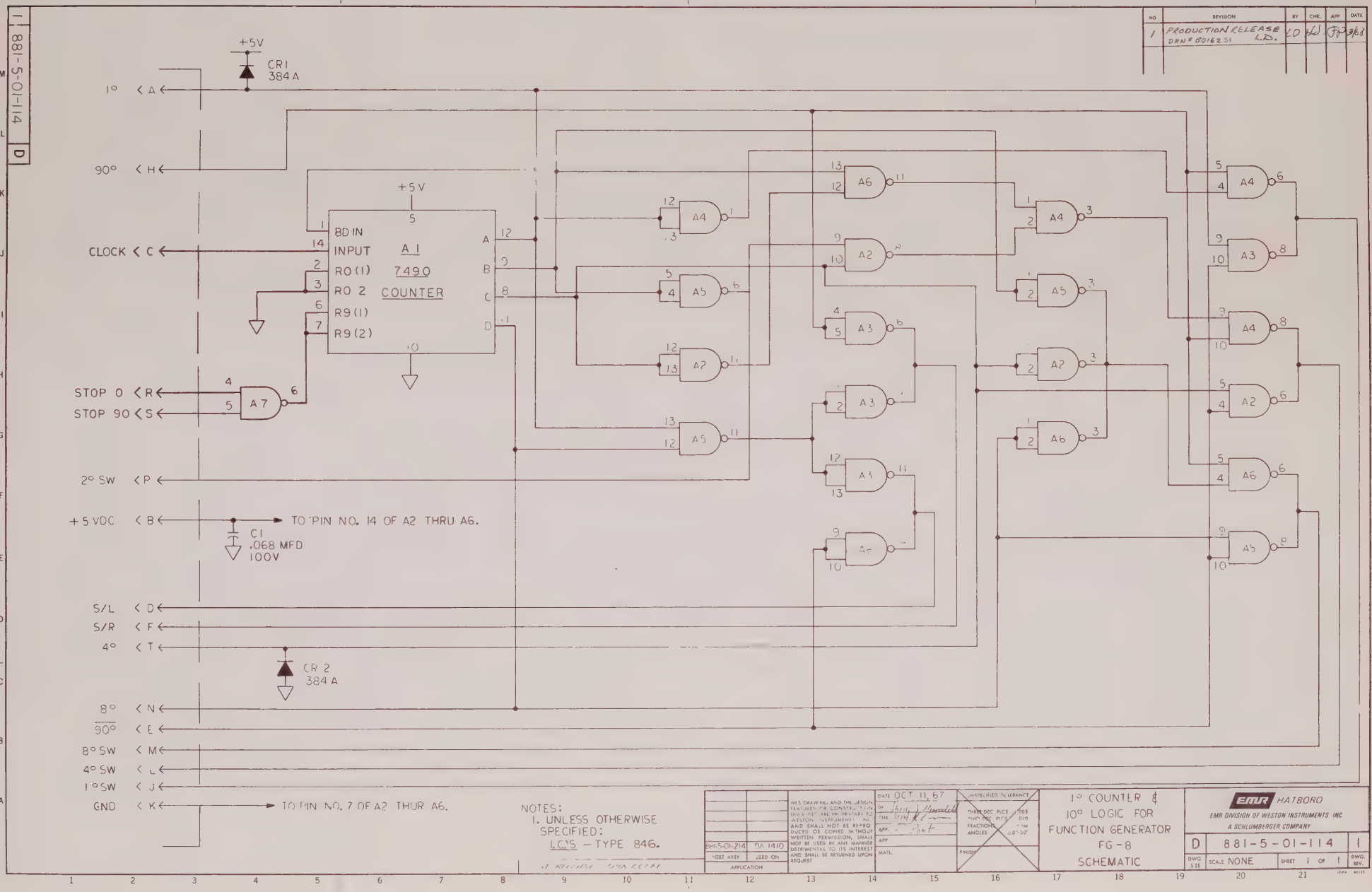
DRIVING LOGIC CIRCUIT, 1° & 0.1° GENERATOR X & Y MULTIPLIERS XYM-2, XYM-5 SCHEMATIC

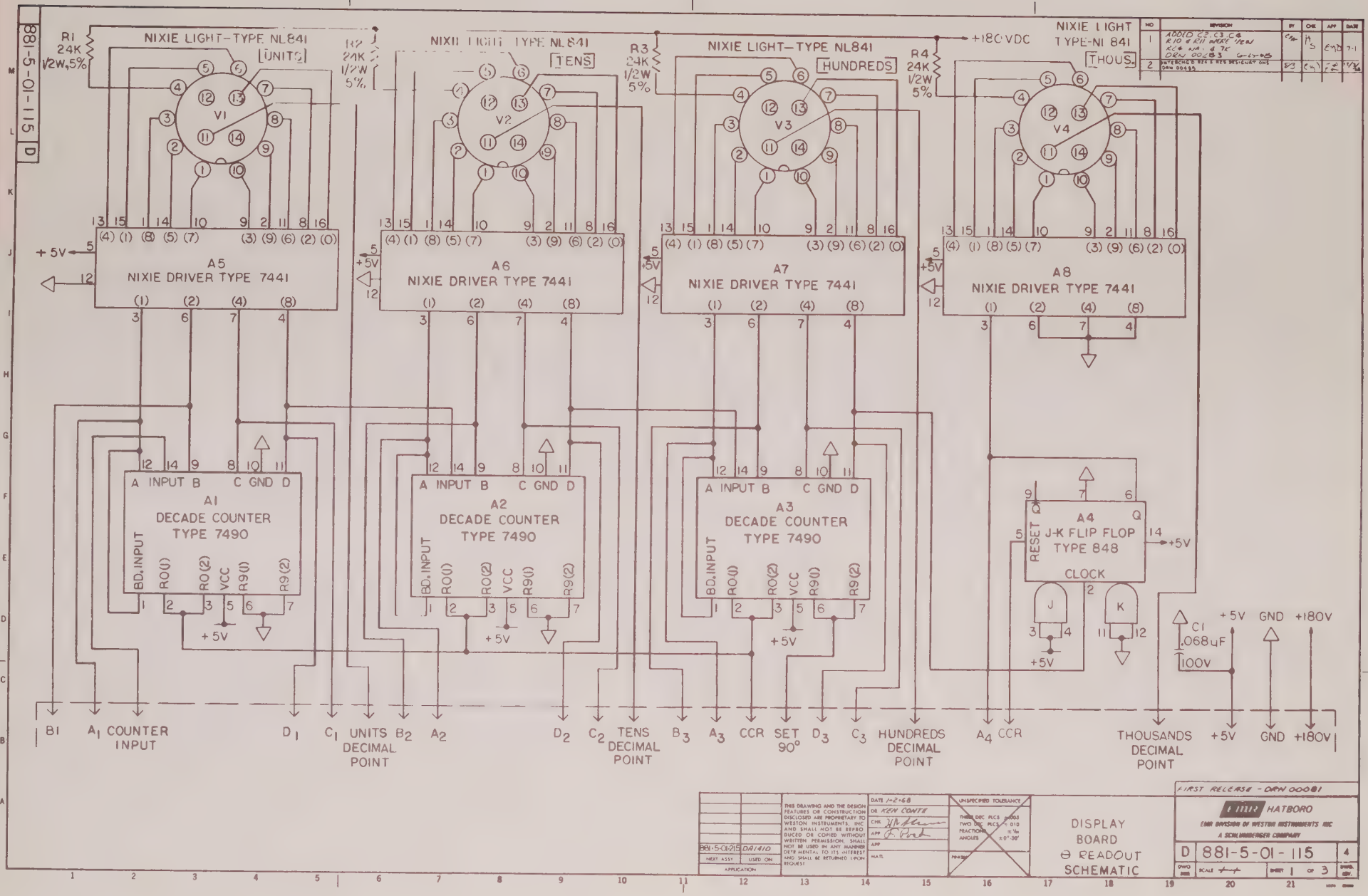
FIRST RELEASE - DRN 00081

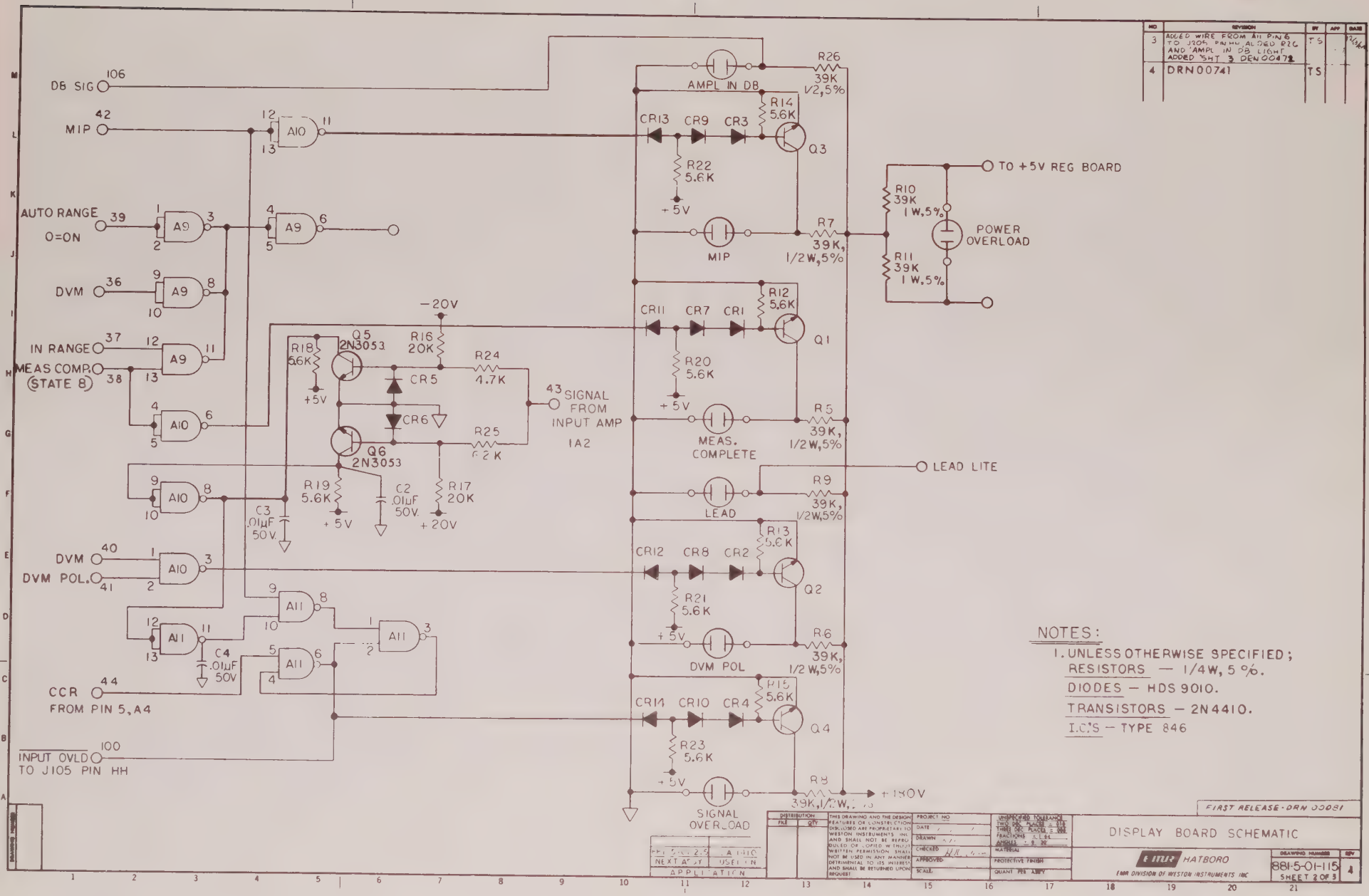
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D	881-5-01-111	1
DWG SIZE	SCALE NONE	SHEET 1 OF 1

DWG. REV.


881-5-01-114 D
NO | REVISION | BY | CHK. | APP | DATE
1 | PRODUCTION RELEASE DRN # 50162 S1 L.D. | LD | | | 3/68
+5V
CR1 384A
1° A
90° H
CLOCK C
BD IN
INPUT
R0(1)
R0 2
R9(1)
R9(2)
A1 7490 COUNTER
STOP 0 R
STOP 90 S
A7
2° SW P
+5 VDC B
TO PIN NO. 14 OF A2 THRU A6.
C1 .068 MFD 100V
S/L D
S/R F
4° T
CR 2 384A
8° N
90° E
8° SW M
4° SW L
1° SW J
GND K
TO PIN NO. 7 OF A2 THUR A6.
A4
A5
A2
A3
A6
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
I.C.'S — TYPE 846.
DATE OCT. 11, 67
DR
CHK
APP.
APP
MATL
FINISH
UNSPECIFIED TOLERANCE
THREE DEC PLCS ±.005
TWO DEC PLCS ±.010
FRACTIONS ±1/64
ANGLES ±0°-30'
1° COUNTER & 10° LOGIC FOR FUNCTION GENERATOR FG-8 SCHEMATIC
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
D 881-5-01-114 1
SCALE NONE
SHEET 1 OF 1


881-5-01-115 D
R1 24K 1/2W,5%
NIXIE LIGHT-TYPE NL841 [UNITS]
R2 24K 1/2W 5%
NIXIE LIGHT-TYPE NL841 [TENS]
R3 24K 1/2W 5%
NIXIE LIGHT-TYPE NL841 [HUNDREDS]
R4 24K 1/2W 5%
+180 VDC
NIXIE LIGHT TYPE-NL 841 [THOUS.]
V1
V2
V3
V4
A5 NIXIE DRIVER TYPE 7441
A6 NIXIE DRIVER TYPE 7441
A7 NIXIE DRIVER TYPE 7441
A8 NIXIE DRIVER TYPE 7441
+5V
A1 DECADE COUNTER TYPE 7490
A2 DECADE COUNTER TYPE 7490
A3 DECADE COUNTER TYPE 7490
A INPUT B C GND D
BD. INPUT
RO(1) RO(2) VCC R9(1) R9(2)
A4 J-K FLIP FLOP TYPE 848
RESET
CLOCK
J
K
C1 .068uF 100V
+5V GND +180V
B1 A1 COUNTER INPUT
D1 C1 UNITS DECIMAL POINT
B2 A2 D2 C2 TENS DECIMAL POINT
B3 A3 CCR SET 90° D3 C3 HUNDREDS DECIMAL POINT
A4 CCR
THOUSANDS DECIMAL POINT
+5V GND +180V
REVISION
ADDED C3, C3, C4 R10 & R11 WERE 1K W R14 WAS 4.7K DRN 00283
DRN 00433
FIRST RELEASE - DRN 00081
DATE 1-2-68
DR KEN CONTE
CHK
APP
MATL
UNSPECIFIED TOLERANCE
THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION. SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST
881-5-01-215 DA1410
NEXT ASSY USED ON
APPLICATION
DISPLAY BOARD & READOUT SCHEMATIC
HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
D 881-5-01-115 4
SCALE
SHEET 1 OF 3



NOTES:

1. UNLESS OTHERWISE SPECIFIED;
   RESISTORS — 1/4W, 5%.
   DIODES — HDS 9010.
   TRANSISTORS — 2N4410.
   I.C.'S — TYPE 846

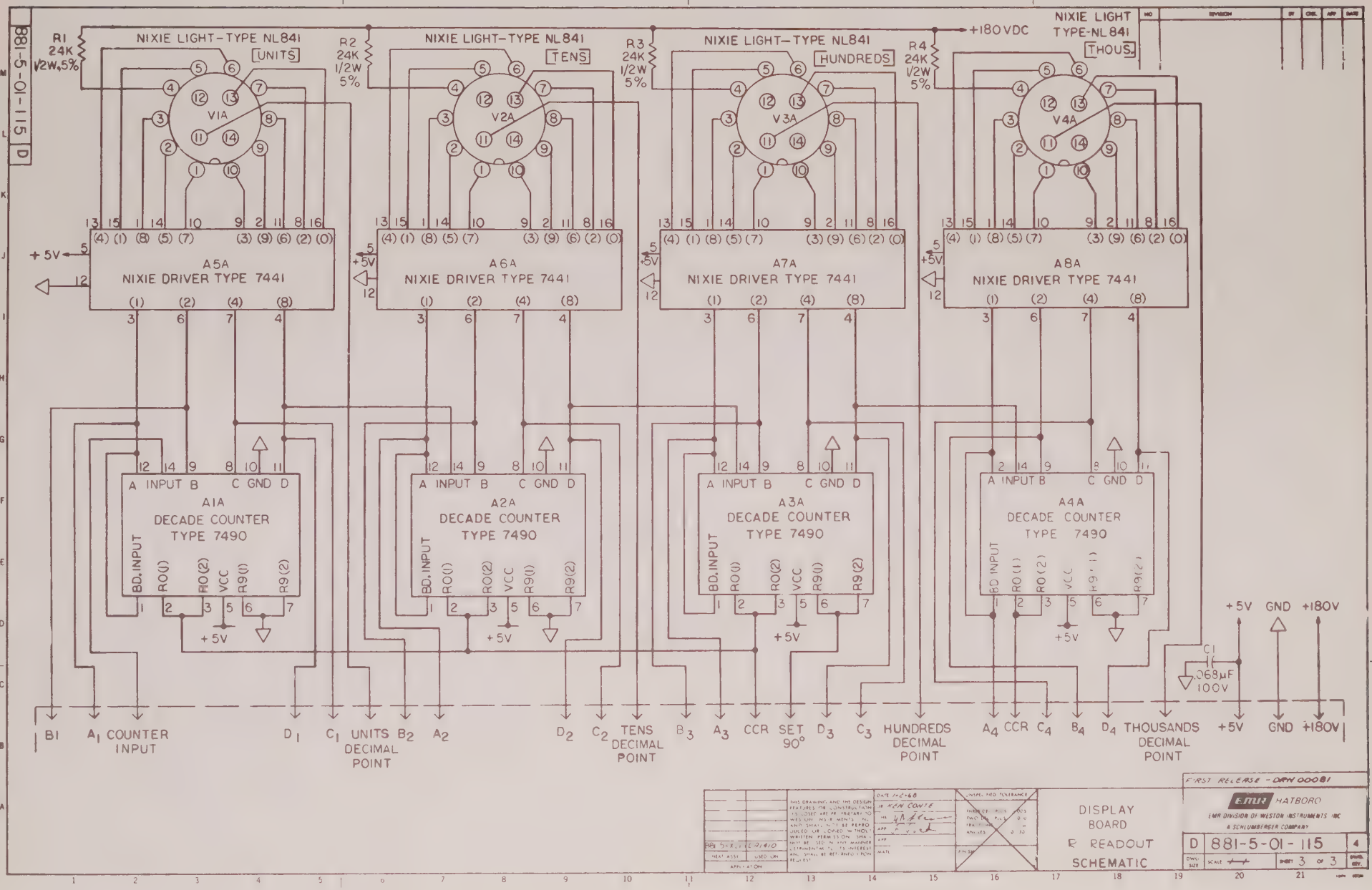
NO	REVISION	BY	APP	DATE
3	ADDED WIRE FROM A11 PIN 6 TO J104 PIN HH, ADDED R26 AND AMPL IN DB LIGHT. ADDED SHT 3 DRN 00472	TS		
4	DRN 00741	TS		

FIRST RELEASE - DRN 00081

DISPLAY BOARD SCHEMATIC

HATBORO — A DIVISION OF WESTON INSTRUMENTS INC

DRAWING NUMBER 881-5-01-115 SHEET 2 OF 3 REV 4


D 881-5-10-115 D
R1 24K 1/2W,5%
R2 24K 1/2W 5%
R3 24K 1/2W 5%
R4 24K 1/2W 5%
+180VDC
NIXIE LIGHT-TYPE NL841 [UNITS]
NIXIE LIGHT-TYPE NL841 [TENS]
NIXIE LIGHT-TYPE NL841 [HUNDREDS]
NIXIE LIGHT TYPE-NL841 [THOUS.]
V1A
V2A
V3A
V4A
+5V
A5A NIXIE DRIVER TYPE 7441
A6A NIXIE DRIVER TYPE 7441
A7A NIXIE DRIVER TYPE 7441
A8A NIXIE DRIVER TYPE 7441
A1A DECADE COUNTER TYPE 7490
A2A DECADE COUNTER TYPE 7490
A3A DECADE COUNTER TYPE 7490
A4A DECADE COUNTER TYPE 7490
A INPUT B C GND D
BD. INPUT R0(1) R0(2) VCC R9(1) R9(2)
C1 .068µF 100V
+5V GND +180V
B1 A1 COUNTER INPUT
D1 C1 UNITS DECIMAL POINT
B2 A2 D2 C2 TENS DECIMAL POINT
B3 A3 CCR SET 90° D3 C3 HUNDREDS DECIMAL POINT
A4 CCR C4 B4 D4 THOUSANDS DECIMAL POINT
+5V GND +180V

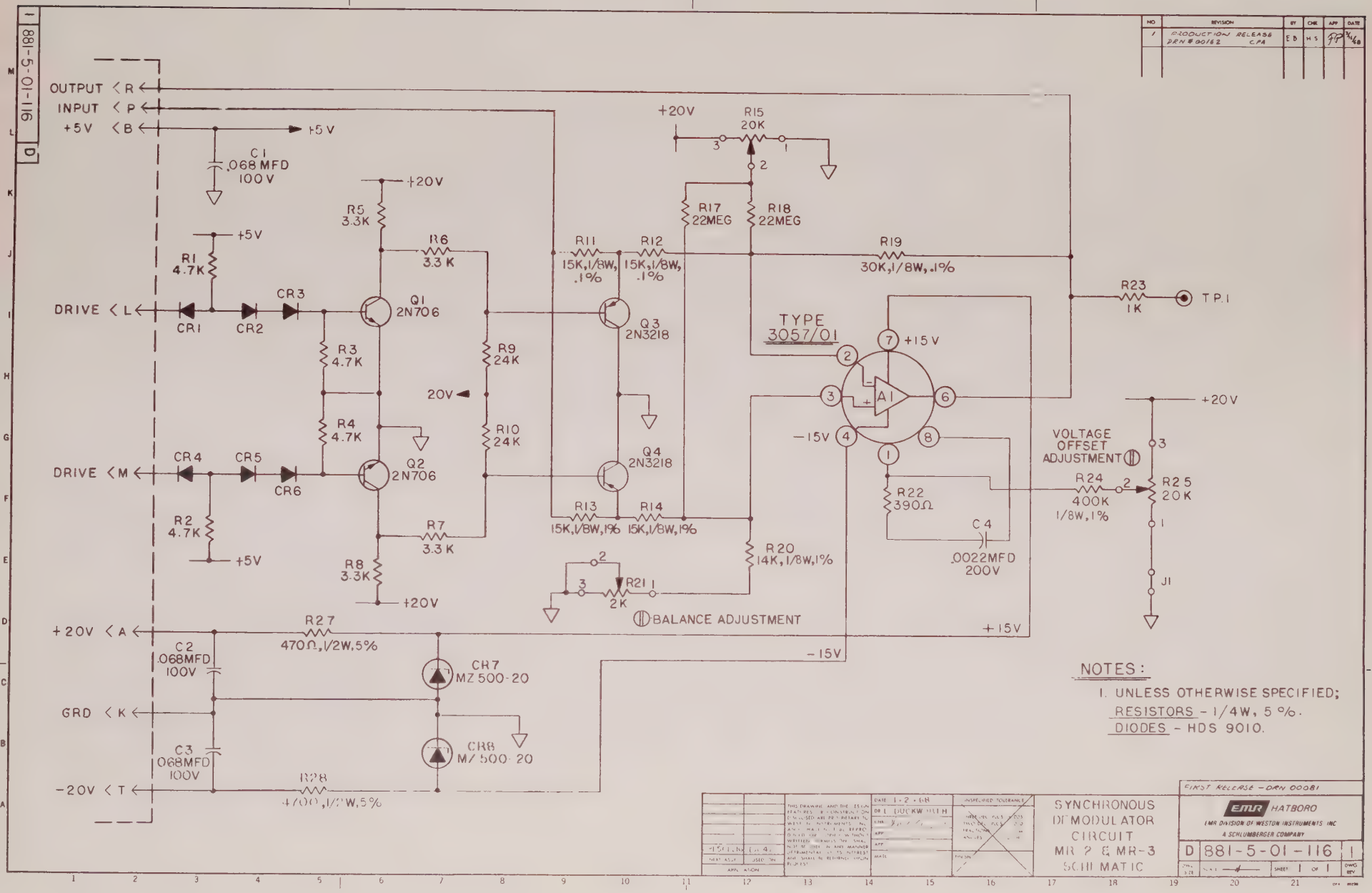
DISPLAY BOARD & READOUT SCHEMATIC

FIRST RELEASE - DAN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D 881-5-01-115 4

SHEET 3 OF 3



NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN # 00182 C/A	E B	H S	JP	3/4/68

NOTES:

1. UNLESS OTHERWISE SPECIFIED;
   RESISTORS - 1/4W, 5 %.
   DIODES - HDS 9010.

FIRST RELEASE - DRN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

SYNCHRONOUS DEMODULATOR CIRCUIT MR 2 & MR-3 SCHEMATIC

D 881-5-01-116 1

SHEET 1 OF 1

NO.	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN #00162 A.L.D.	E.B.	H.S.	[illegible]	3/4/68

881-5-01-117 D

40 OR 80 <R
40 OR 80 <N
30 OR 70 <L
30 OR 70 <J
20 OR 60 <H
20 OR 60 <E
10 OR 50 <D
10 OR 50 <C

A1 A2 A3 A4
RESET SET
TYPE 848

+5V
CR2 384A
CR1 384A

INTER-SHIFT REG. SIGNAL <A
RESET <S
SR <F
CLOCK <T
SL <M
INTER-SHIFT REG. SIGNAL <P
+5V DC <B ► +5V TO PIN 14 OF A1 THRU A4.
C1 .068 MFD 100V
GND <K ► GND TO PIN 7 OF A1 THRU A4.

FIRST RELEASE - DRN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

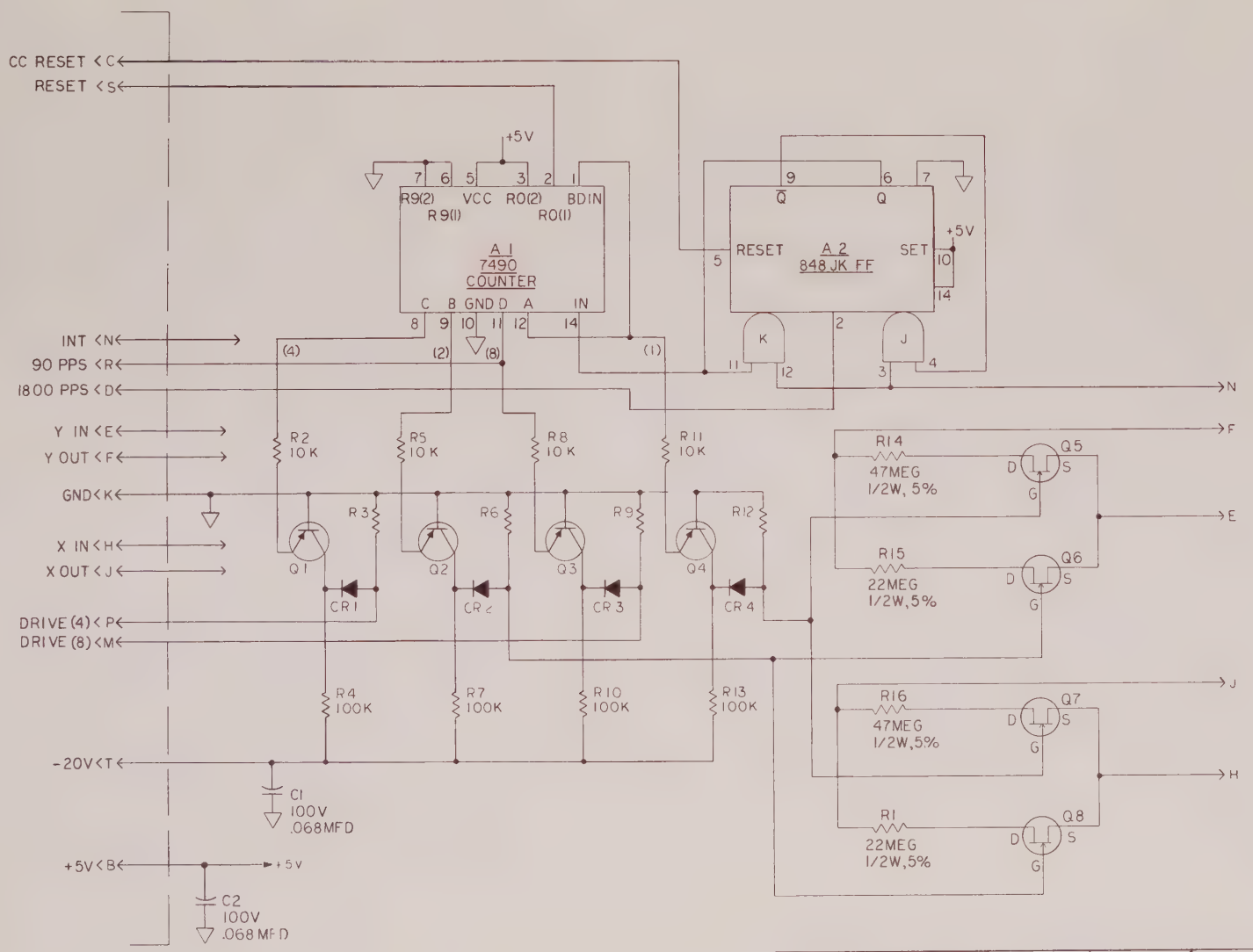
SHIFT REGISTER
CIRCUIT (1/2 REGISTER)
FOR FG6, FG7, XYM3, XYM4
SCHEMATIC

D 881-5-01-117 1

SCALE: 4/1 SHEET 1 OF 1

THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION. SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST

DATE 29/12/67
UNSPECIFIED TOLERANCE
THREE DEC. PLCS ±.005
TWO DEC. PLCS ±.010
FRACTIONS ±1/64
ANGLES ±0°30'
FINISH



NO.	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN # 00162	E.B	H.S.	FP	3/14/68

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTORS - 1/4 W, 5%.
   DIODES - HDS 9010.
2. TRANSISTORS: Q1 THRU Q4 ARE 2N4121; Q5 THRU Q8 ARE SFB4832.
3. RESISTORS R3 R6 R9 & R12 ARE 390K.

FIRST RELEASE - DRN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

INTEGRATOR BUFFER DRIVE CIRCUIT (1-10WT) 1-B2 SCHEMATIC

D 881-5-01-118 1

DWG SIZE D | SCALE NONE | SHEET 1 OF 1 | DWG REV

DATE 21 SEPT. 67

UNSPECIFIED TOLERANCE: THREE DEC. PLCS ±.005, TWO DEC. PLCS ±.010, FRACT ONE ±1/64, ANGLES ±0°-30'

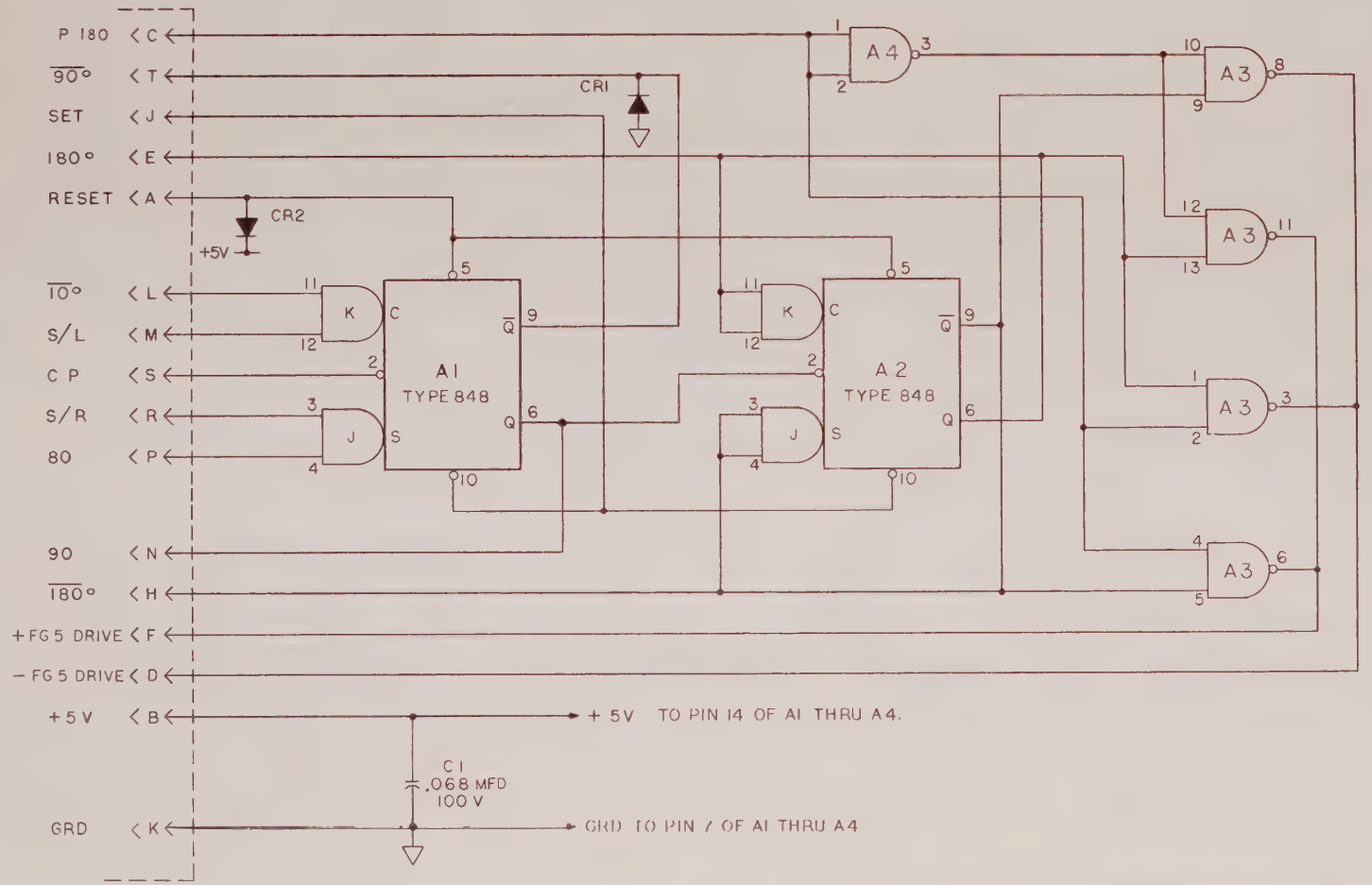
THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC. AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION. IT SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST

881-5-01-118 D

NEXT ASSY | USED ON | APPLICATION | DA 410

NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN #00162 L.D.	E.B.	H.S.	[illegible]	3/1/68

D 611-10-5-188 1



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   DIODES – 384A
   I.C.'S. – TYPE 846.

THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC. AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST

DATE 12-21-67
DR DUCKWORTH
CHK
APP
APP
MATL

UNSPECIFIED TOLERANCE
THREE DEC PLCS .005
TWO DEC PLCS .010
FRACTIONS 1/64
ANGLES 0 30
FINISH

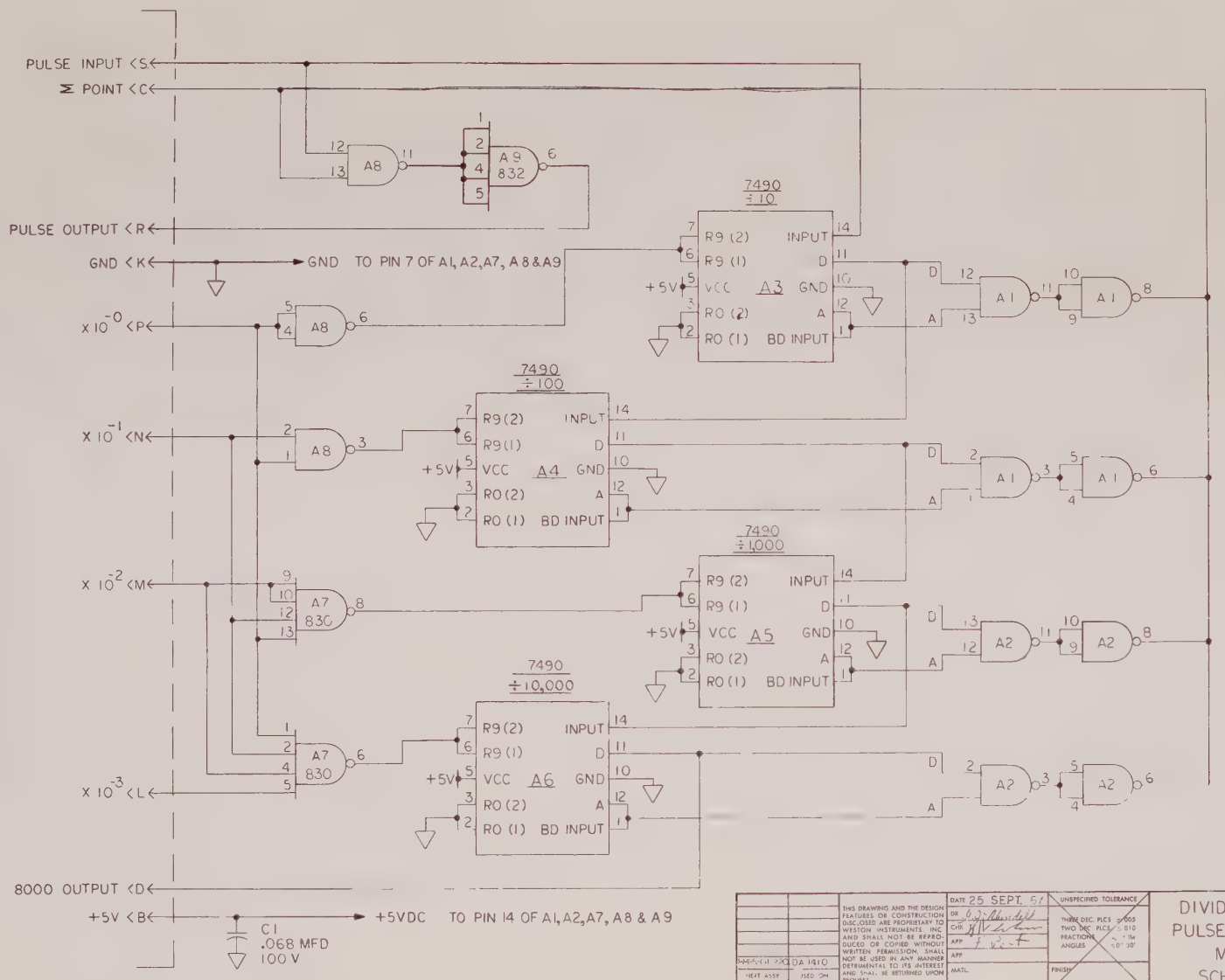
881-5-01-219 DA 1410
NEXT ASSY USED ON
APP. CAT ON

SCHEMATIC DIAGRAM
90° & 180° FF FOR
FUNCTION GENERATOR
I.C. 9, SCHEMATIC

FIRST RELEASE – DRN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

D 881-5-01-119 1
DWG. SIZE | SCALE — | SHEET 1 OF 1 | DWG. REV.



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
I.C'S. – TYPE 846.

NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN # 0016251 A.D.	LD	VD	LS	9/5

FIRST RELEASE – DRN 00081

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DATE 25 SEPT. 67
DR L.J. Abercrombie
CHK
APP
APP
MATL.

UNSPECIFIED TOLERANCE
THREE DEC. PLCS ± .005
TWO DEC PLCS ± .010
FRACTIONS ± 1/64
ANGLES ± 30'
FINISH

DIVIDED CLOCK PULSE CIRCUIT MO-2 SCHEMATIC

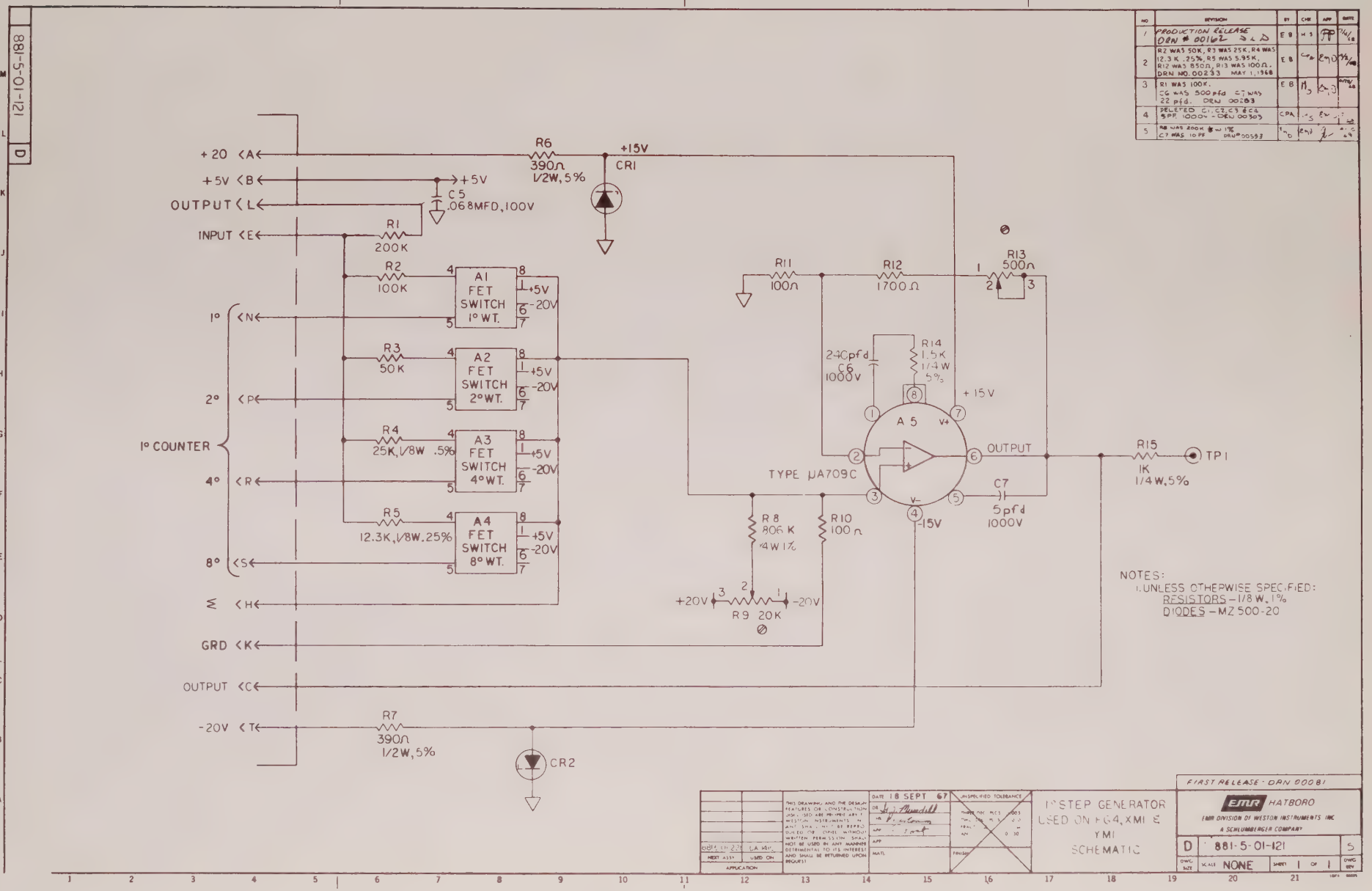
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

D | 881-5-01-120 | 1

DWG SIZE | SCALE NONE | SHEET 1 OF 1 | DWG REV.

NEXT ASSY | USED ON APPLICATION | DA 1410

881-5-01-120 D



NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN # 00162	E B	M S		7/4/68
2	R2 WAS 50K, R3 WAS 25K, R4 WAS 12.3 K .25%, R5 WAS 5.95K, R12 WAS 850Ω, R13 WAS 100Ω. DRN NO. 00233 MAY 1, 1968	E B			
3	R1 WAS 100K. C6 WAS 500pfd C7 WAS 22 pfd. DRN 00283	E B			
4	DELETED C1, C2, C3 & C4 4PF. 1000V - DRN 00303	CPA			
5	R8 WAS 200K C7 WAS 10 PF DRN#00593				

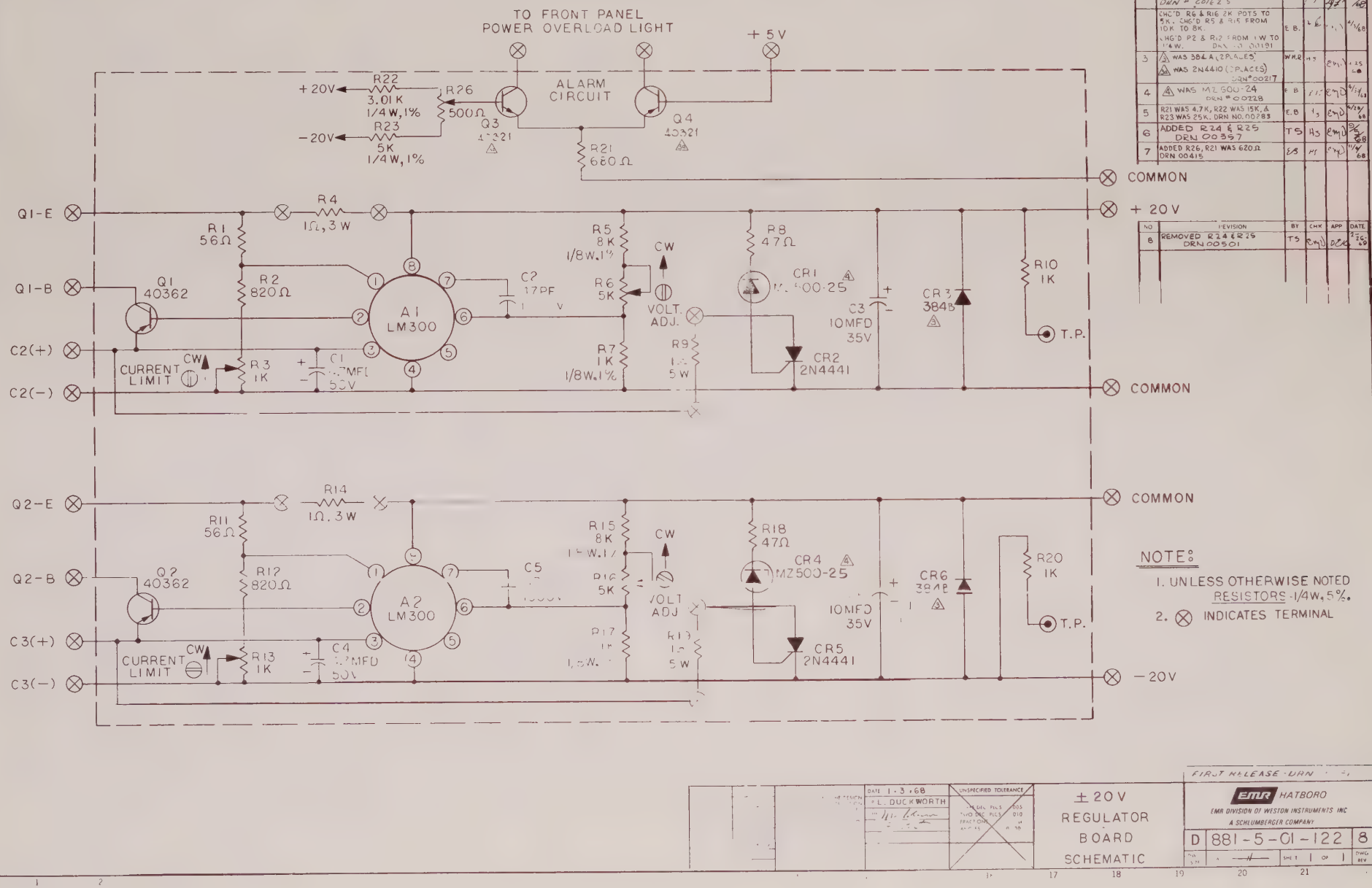
		THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION SHOWN ARE PROPRIETARY TO WESTON INSTRUMENTS IN ANY SHAPE, MUST BE REPRODUCED OR USED FOR OTHER THAN WRITTEN PERMISSION SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST	DATE 18 SEPT 67	UNSPECIFIED TOLERANCE	1° STEP GENERATOR USED ON FG4, XMI & YMI SCHEMATIC

FIRST RELEASE - DRN 00081

EMR HATBORO
A DIVISION OF WESTON INSTRUMENTS INC.
A SCHLUMBERGER COMPANY

D 881-5-01-121 5

DWG SIZE | X ALL | NONE | SHEET 1 OF 1 | DWG REV



NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN # 00625	WB			3/27/68
	CHG'D R6 & R16 2K POTS TO 5K. CHG'D R5 & R15 FROM 10K TO 8K. CHG'D R2 & R12 FROM 1W TO 1/4W. DRN # 00181	E.B.			4/16/68
3	⚠3 WAS 384A (2PLACES) ⚠4 WAS 2N4410 (2PLACES) DRN#00217	W.H.R.			4/25/68
4	⚠4 WAS MZ500-24 DRN # 00228	E.B.			5/13/68
5	R21 WAS 4.7K, R22 WAS 15K, & R23 WAS 25K. DRN NO. 00283	E.B.			5/29/68
6	ADDED R24 & R25 DRN 00357	T.S.			6/28/68
7	ADDED R26, R21 WAS 620Ω DRN 00415	E.B.			11/4/68

NO	REVISION	BY	CHK	APP	DATE
8	REMOVED R24 & R25 DRN 00501	T.S.			7/30/69

NOTES:
1. UNLESS OTHERWISE NOTED RESISTORS 1/4W, 5%.
2. ⊗ INDICATES TERMINAL

DATE 1-3-68
L. DUCKWORTH

UNSPECIFIED TOLERANCE
TWO DEC PLS .010
FRACTIONS

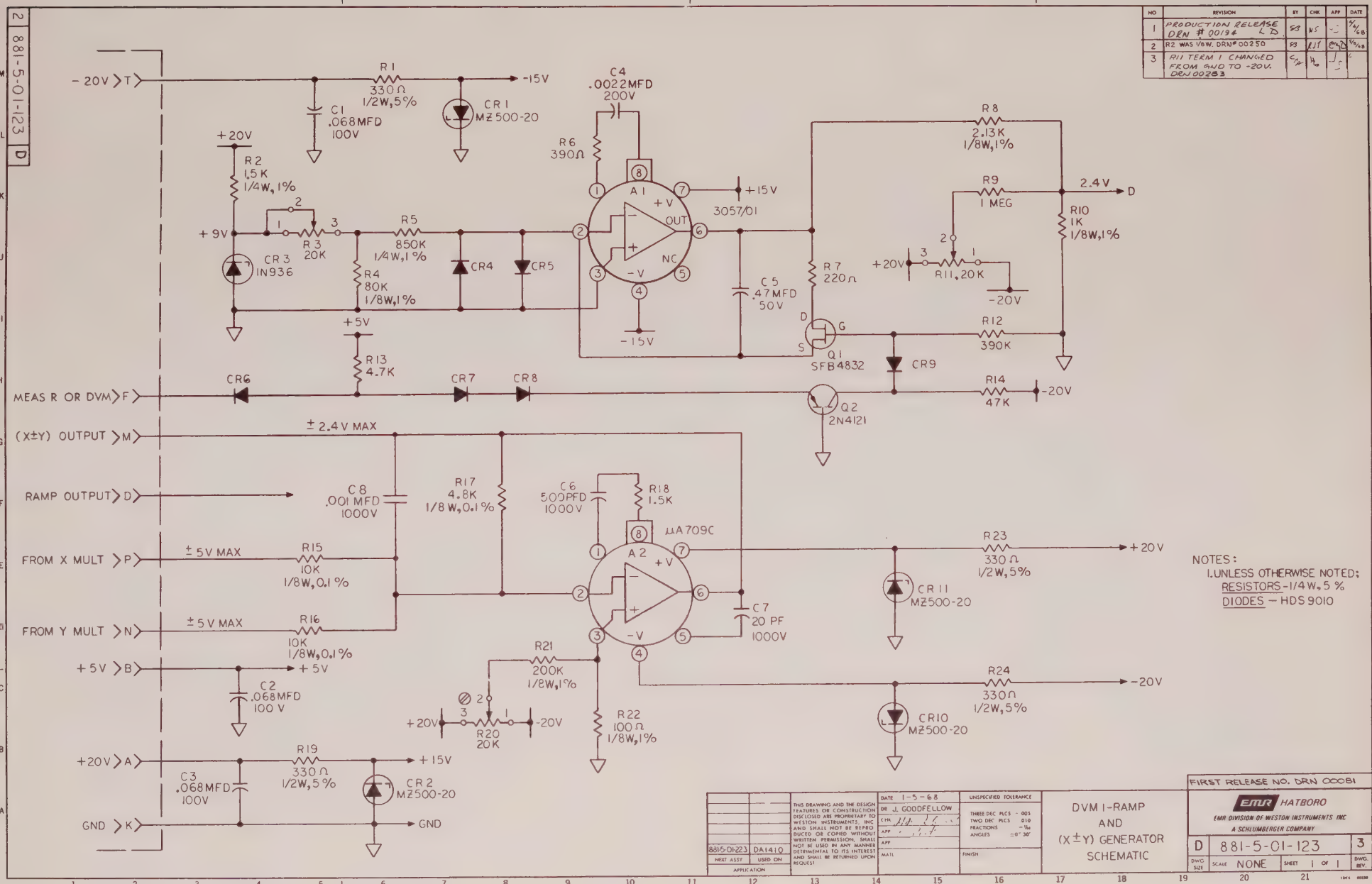
FIRST RELEASE - DRN

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

±20V REGULATOR BOARD SCHEMATIC

D | 881-5-01-122 | 8

SHEET 1 OF 1



NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN # 00194 LD	SB	WS		3/1/68
2	R2 WAS 10W. DRN# 00250	SB	WT		5/10/68
3	R11 TERM 1 CHANGED FROM GND TO -20V. DRN 00283				

NOTES:
1. UNLESS OTHERWISE NOTED:
RESISTORS - 1/4W, 5 %
DIODES — HDS 9010

FIRST RELEASE NO. DRN 00081

8815-01-223 | DA1410
NEXT ASSY | USED ON
APPLICATION

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DATE 1-5-68
DR J. GOODFELLOW
CHK
APP
APP
MAT'L

UNSPECIFIED TOLERANCE
THREE DEC PLCS - .003
TWO DEC PLCS .010
FRACTIONS ± 1/64
ANGLES ±0° 30'
FINISH

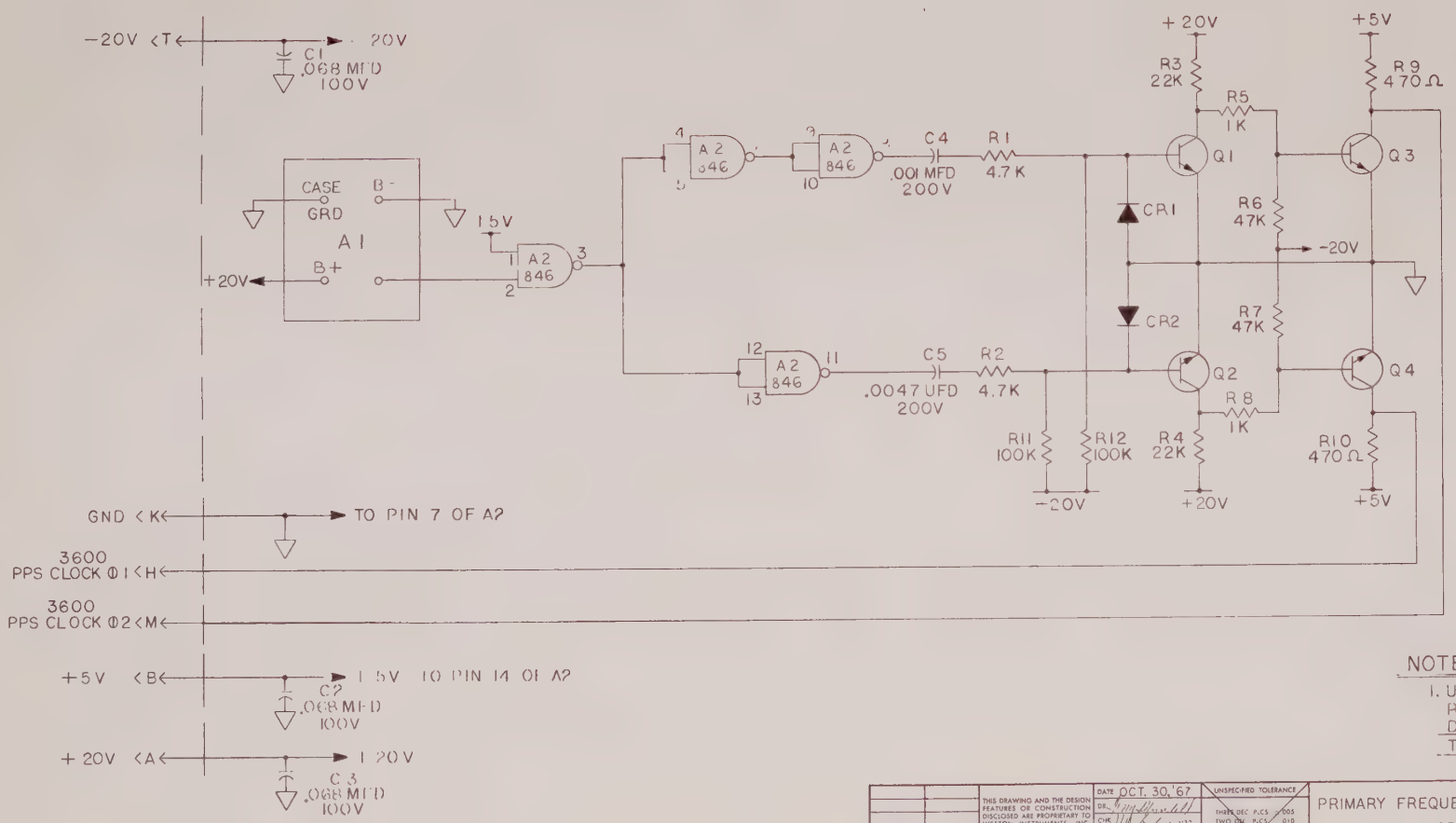
DVM I-RAMP AND (X±Y) GENERATOR SCHEMATIC

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D | 881-5-01-123 | 3
DWG SIZE | SCALE NONE | SHEET 1 OF 1 | DWG. REV.

NO.	REVISION	BY	CHK	APP.	DATE
1	PRODUCTION RELEASE DRN #00162 D.L.D.	E.B.	H.S.	FP	3/4/68

881-5-01-124 D



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTORS — 1/4W, 5%.
   DIODES — HDS 9010.
   TRANSISTORS 2N3904.

FIRST RELEASE-DRN 00081

THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC. AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION, SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST

DATE	OCT. 30, '67
DR.	
CHK.	
APP.	
APP.	
MATL.	

UNSPECIFIED TOLERANCE: THREE DEC. PLCS .005; TWO DEC. PLCS .010; FRACTIONS 1/64; ANGLES 0°30'; FINISH

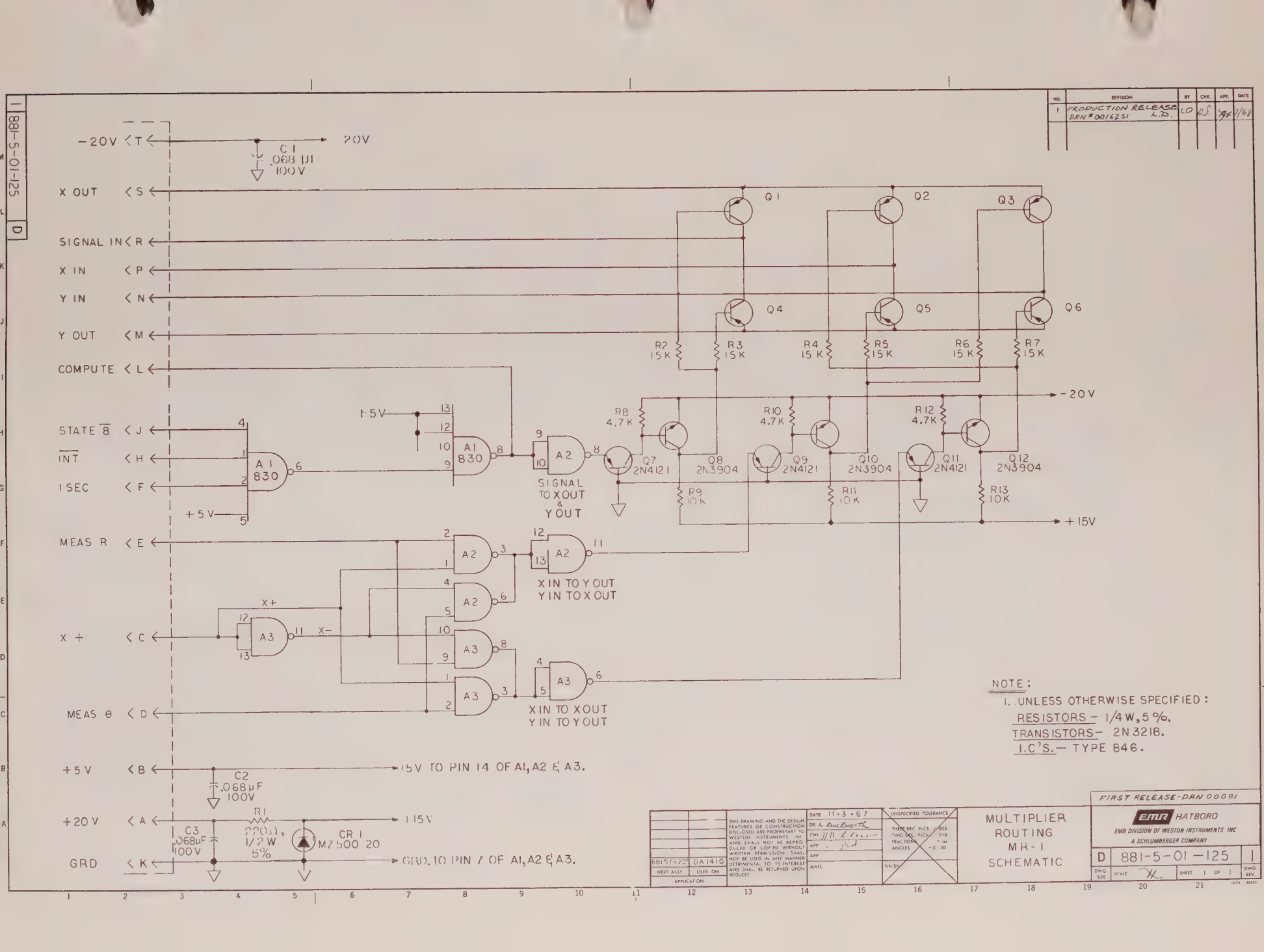
PRIMARY FREQUENCY GENERATOR
FR-I
SCHEMATIC

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D | 881-5-01-124 | 1

DWG SIZE | SCALE NONE | SHEET 1 OF 1 | DWG REV.

NEXT ASSY | USED ON | APPLICATION



NOTE:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTORS – 1/4W, 5%.
   TRANSISTORS – 2N3218.
   I.C'S. – TYPE 846.

NO.	REVISION	BY	CHK.	APP.	DATE
1	PRODUCTION RELEASE DRN # 0016251 A.D.	LD	HS		9/1/68

881-5-01-125	DA 1410	DATE 11-3-67	UNSPECIFIED TOLERANCE: THREE DEC PLCS ±.005, TWO DEC PLCS ±.010, FRACTIONS ±1/64, ANGLES ±0°30'
NEXT ASSY.	USED ON	DR L. Duckworth	
APPLICATION		CHK	
		APP	
		APP	
		MATL	

THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS INC AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION. SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST

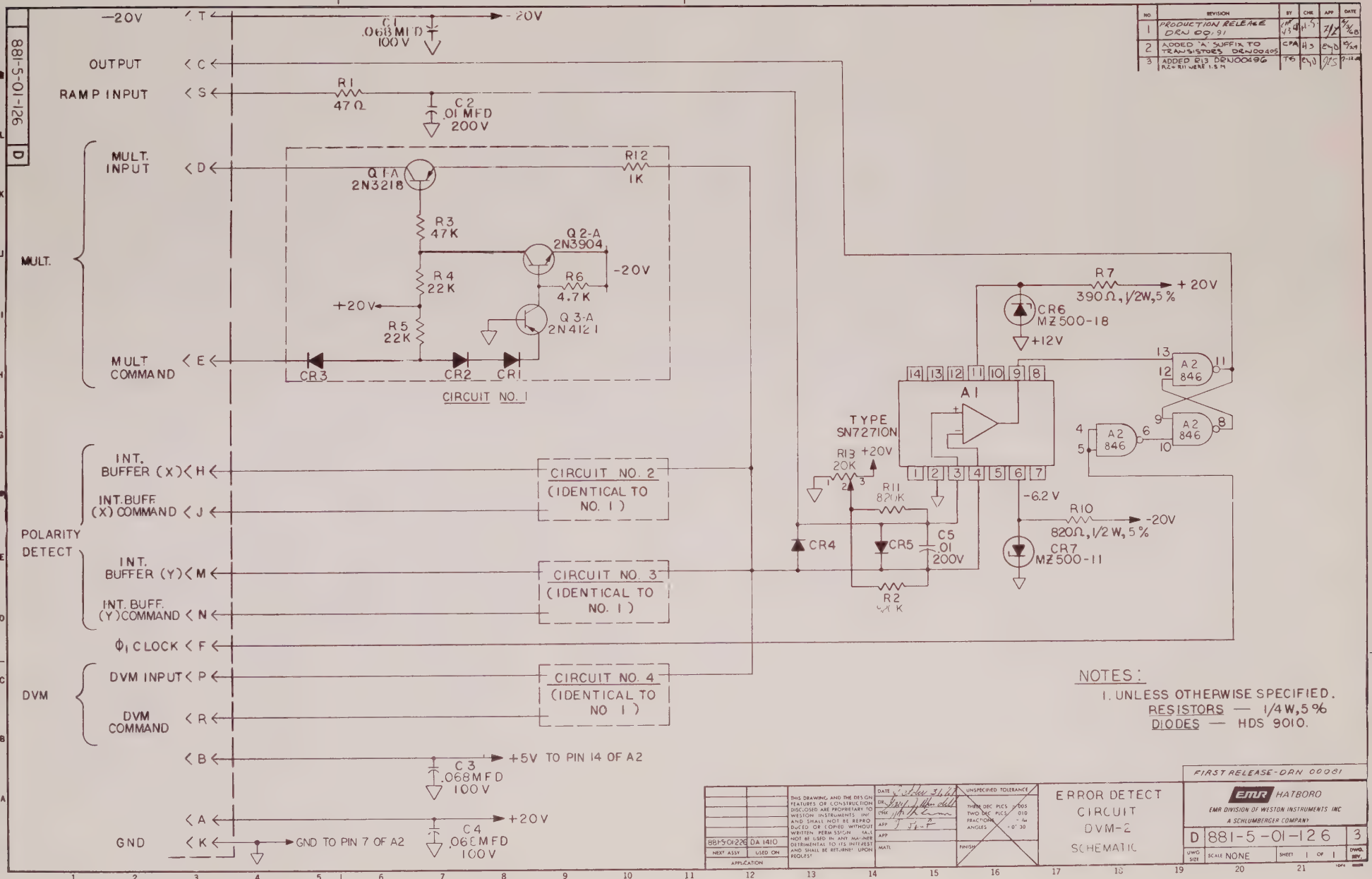
MULTIPLIER ROUTING MR-1 SCHEMATIC

FIRST RELEASE-DRN 00081

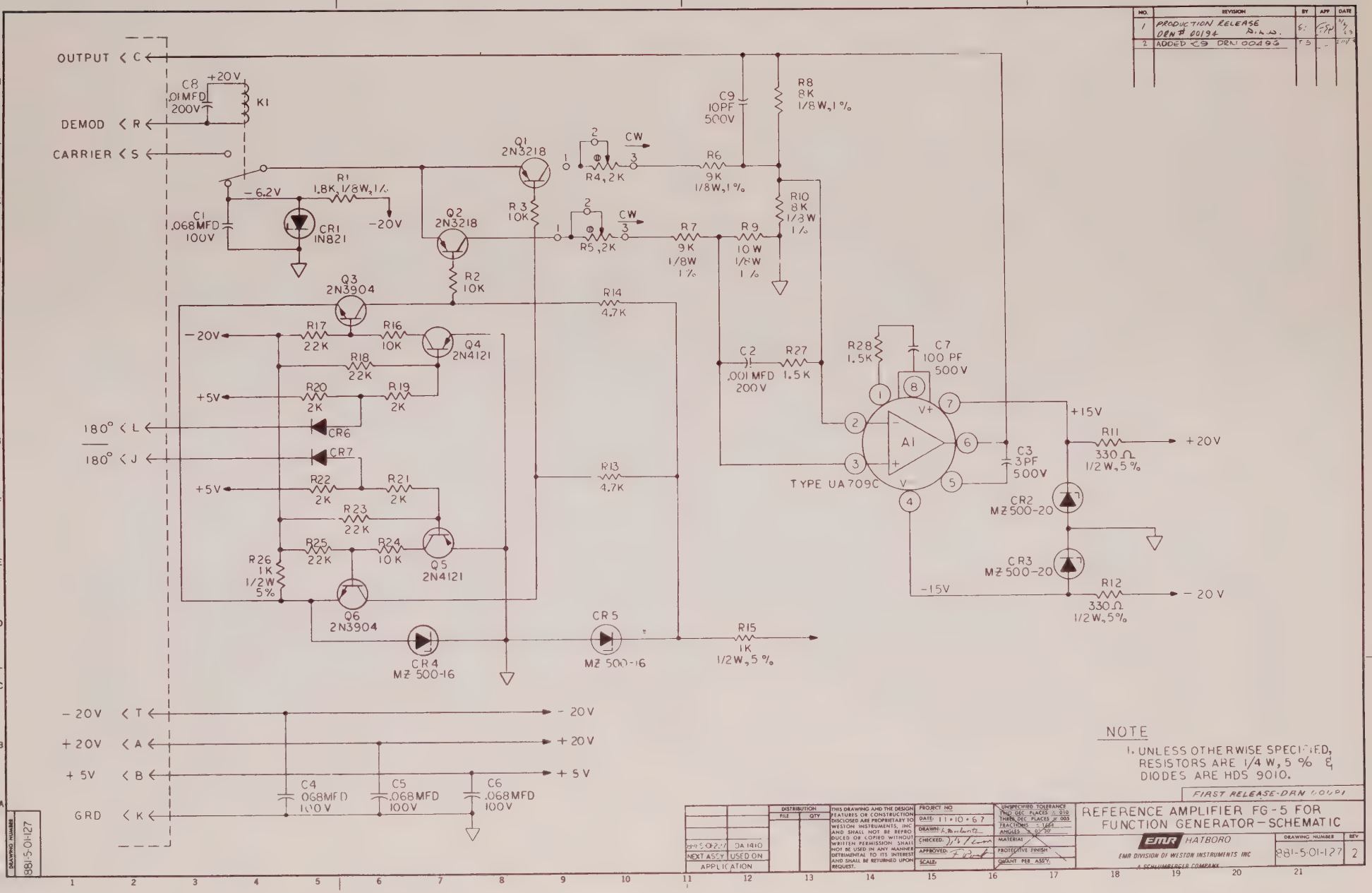
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D | 881-5-01-125 | 1

DWG SIZE D | SCALE 1/4 | SHEET 1 OF 1 | DWG REV. 1



NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN 00091				
2	ADDED 'A' SUFFIX TO TRANSISTORS DRN00405	CPA	HS		
3	ADDED R13 DRN00496 R2 & R11 WERE 1.5M	TG			



NO.	REVISION	BY	APP	DATE
1	PRODUCTION RELEASE DRN # 00194 D.L.W.	B:	FSP	3/4/69
2	ADDED C9 DRN 00495	FS	-	2/17/7

NOTE

1. UNLESS OTHERWISE SPECIFIED, RESISTORS ARE 1/4 W, 5 % & DIODES ARE HDS 9010.

FIRST RELEASE-DRN 00091

DISTRIBUTION: FILE / QTY	THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION. SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST.	PROJECT NO	UNSPECIFIED TOLERANCE: TWO DEC PLACES ± .010; THREE DEC PLACES ± .005; FRACTIONS ± 1/64; ANGLES ± 0° 30'
		DATE: 11-10-67	
		DRAWN: K. Bernhardt	MATERIAL
		CHECKED: D/L/Lewis	PROTECTIVE FINISH
		APPROVED: F. Pinkerton	
		SCALE:	QUANT PER ASS'Y.

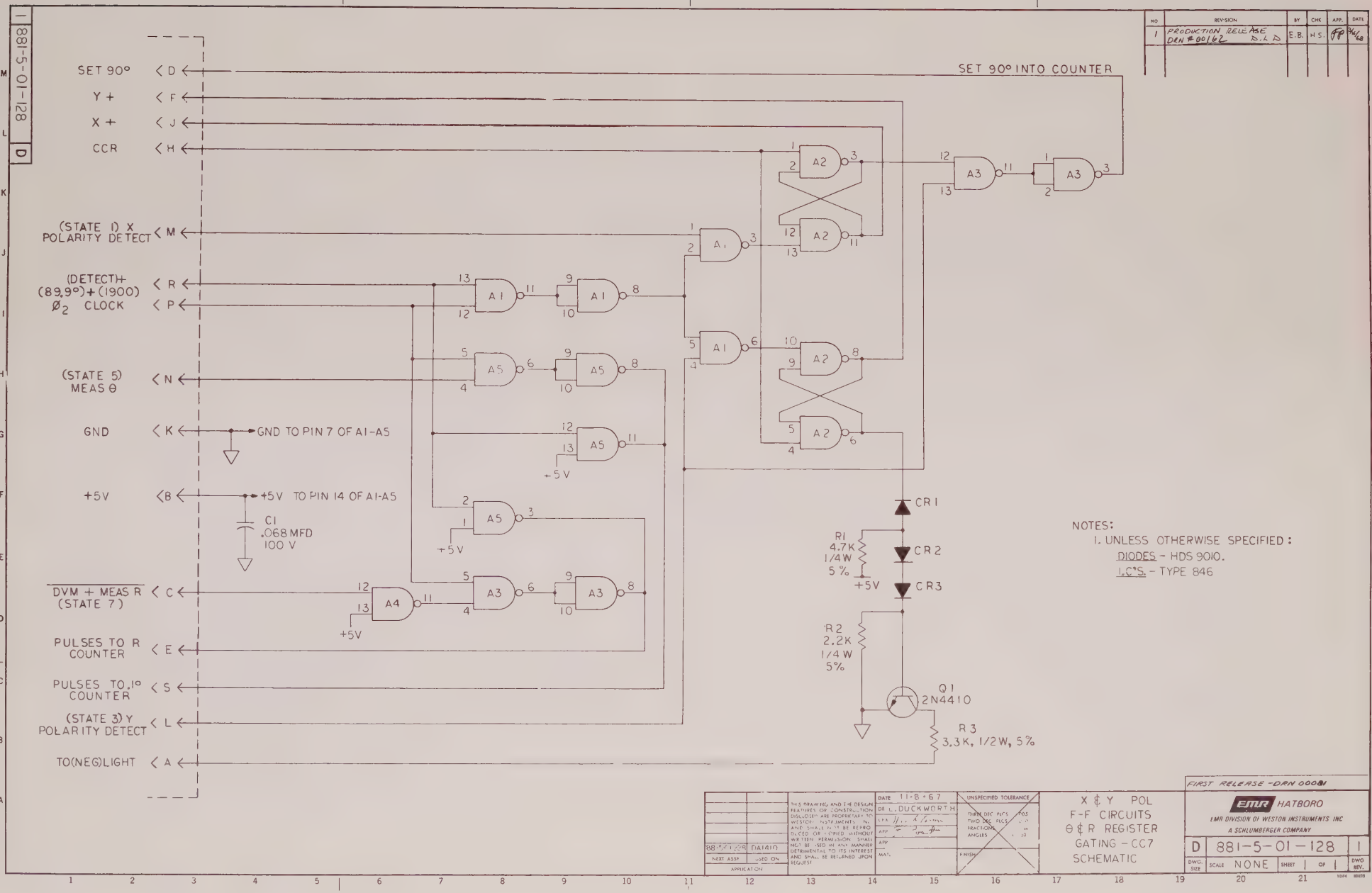
REFERENCE AMPLIFIER FG-5 FOR FUNCTION GENERATOR—SCHEMATIC

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

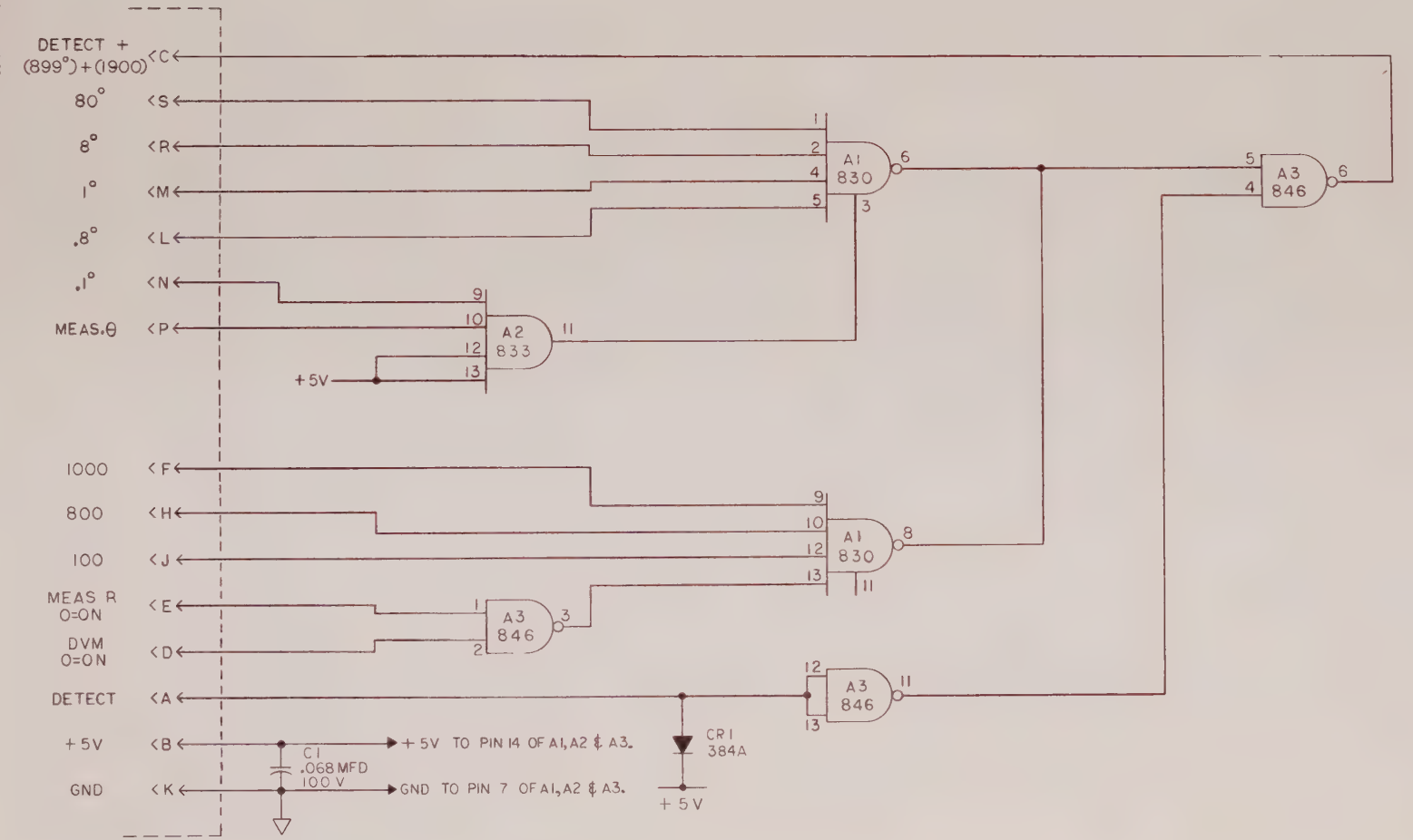
DRAWING NUMBER 881-5-01-127 REV 2

DRAWING NUMBER 881-5-01-127

NEXT ASSY | USED ON | APPLICATION | DA 1410


881-5-01-128 D
SET 90°
Y +
X +
CCR
(STATE 1) X POLARITY DETECT
(DETECT)+ (89.9°)+(1900) Ø2 CLOCK
(STATE 5) MEAS θ
GND
GND TO PIN 7 OF A1-A5
+5V
+5V TO PIN 14 OF A1-A5
C1 .068 MFD 100 V
DVM + MEAS R (STATE 7)
PULSES TO R COUNTER
PULSES TO .1° COUNTER
(STATE 3) Y POLARITY DETECT
TO(NEG)LIGHT
SET 90° INTO COUNTER
A1
A2
A3
A4
A5
CR1
CR2
CR3
R1 4.7K 1/4W 5%
R2 2.2K 1/4W 5%
R3 3.3K, 1/2W, 5%
Q1 2N4410
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
DIODES - HDS 9010.
I.C'S. - TYPE 846
X & Y POL
F-F CIRCUITS
θ & R REGISTER
GATING - CC7
SCHEMATIC
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
D 881-5-01-128 1
FIRST RELEASE - DRN 00081

NO.	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN#-00162 D.L.D.	E B	H.S.		3/1/68



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DATE 12-21-67
DR ACN CONTI
CHK
APP
APP
MAT'L
UNSPECIFIED TOLERANCE
THREE DEC PLCS ±.005
TWO DEC PLCS ±.010
FRACTIONS ±1/64
ANGLES 0 30'
FINISH
NEXT ASSY
USED ON
APPLICATION

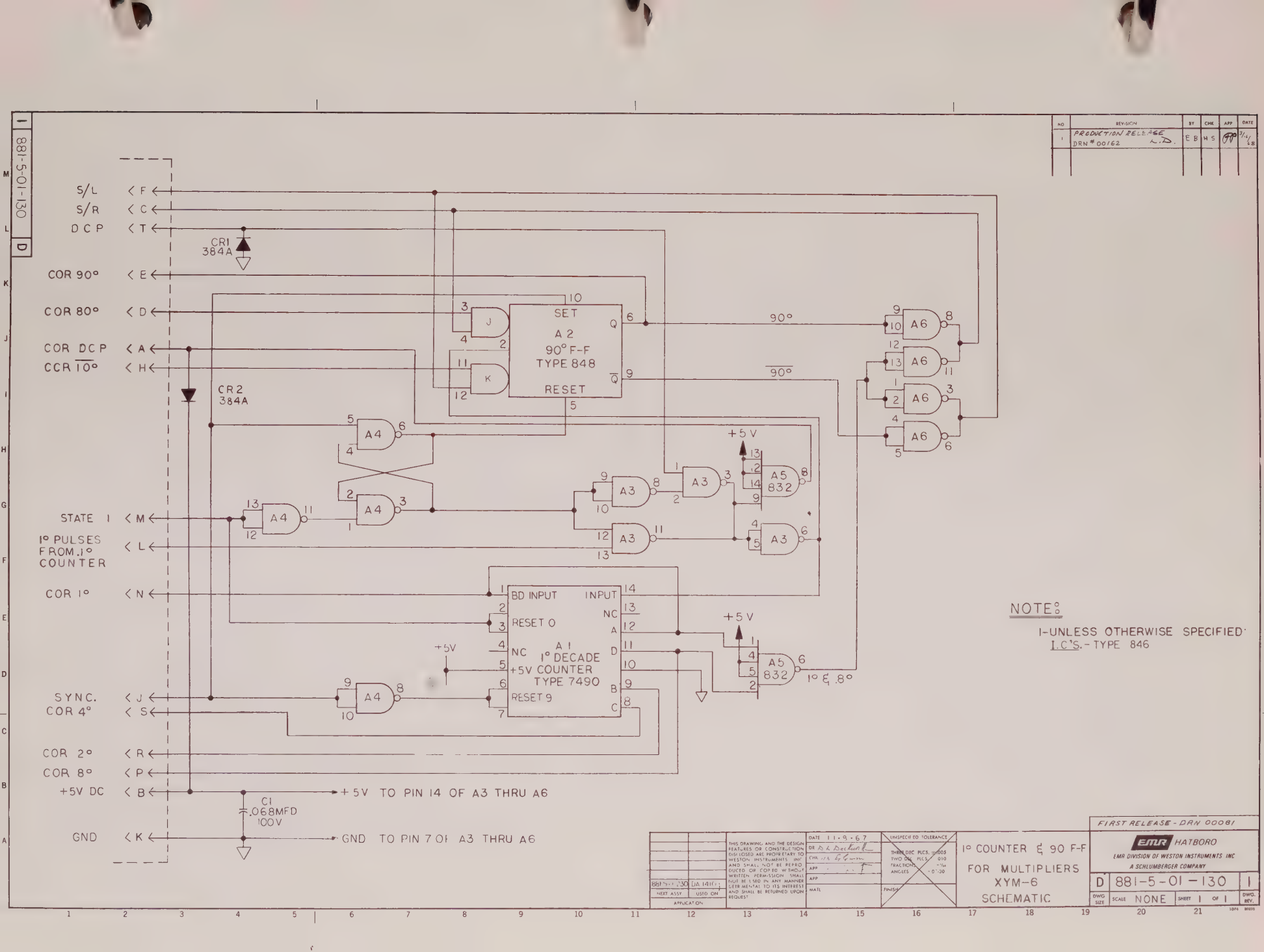
DETECT SWITCHING LOGIC CC-9 SCHEMATIC

FIRST RELEASE-DRN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

D | 881-5-01-129 | 1
DWG SIZE | SCALE 1/1 | SHEET 1 OF 1 | DWG REV

881-5-01-129 D


881-5-01-130
D
NO
REVISION
BY
CHK
APP
DATE
1
PRODUCTION RELEASE
DRN # 00162
E B
H S
3/1/68
S/L
S/R
D C P
COR 90°
COR 80°
COR DCP
CCR 10°
STATE 1
1° PULSES FROM .1° COUNTER
COR 1°
SYNC.
COR 4°
COR 2°
COR 8°
+5V DC
GND
CR1 384A
CR2 384A
C1 .068MFD 100V
+5V TO PIN 14 OF A3 THRU A6
GND TO PIN 7 OF A3 THRU A6
A2 90° F-F TYPE 848
SET
RESET
A1 1° DECADE +5V COUNTER TYPE 7490
BD INPUT
RESET 0
RESET 9
NC
90°
1° & .8°
+5V
A3
A4
A5 832
A6
NOTES
1-UNLESS OTHERWISE SPECIFIED
I.C'S.- TYPE 846
FIRST RELEASE - DAN 00081
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
1° COUNTER & 90 F-F
FOR MULTIPLIERS
XYM-6
SCHEMATIC
D 881-5-01-130 1
SCALE NONE
SHEET 1 OF 1
DWG. REV.
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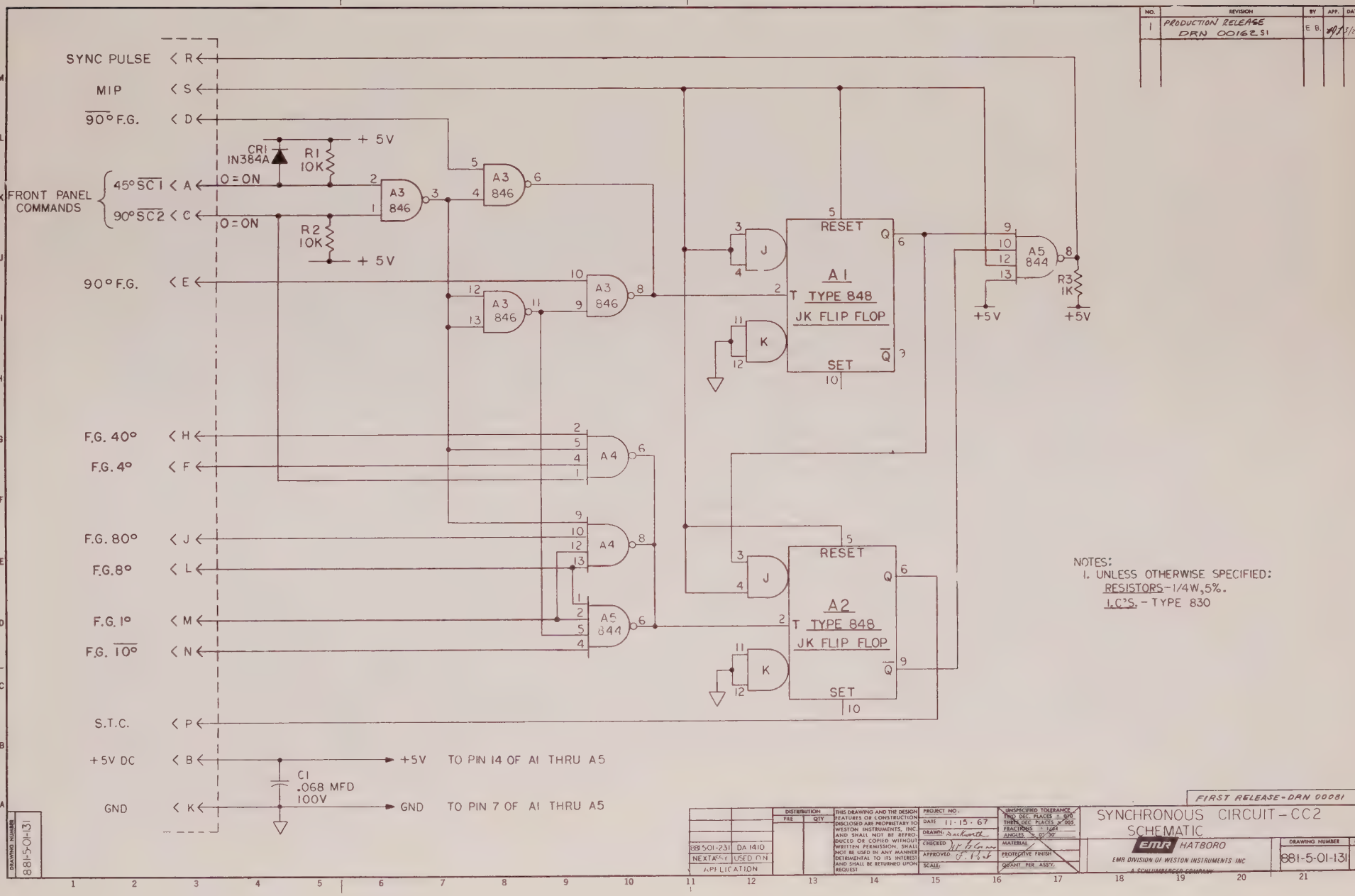
DATE 11-9-67
DR R.L. Beckwith
CHK
APP
APP
MATL
UNSPECIFIED TOLERANCE
THREE DEC PLCS ±.005
TWO DEC PLCS ±.010
FRACTIONS ±1/64
ANGLES ±0°30'
FINISH
NEXT ASSY
USED ON
APPLICATION



NO.	REVISION	BY	APP.	DATE
1	PRODUCTION RELEASE DRN 001625 1	E.B.		4/13/68

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
RESISTORS - 1/4W, 5%.
I.C'S. - TYPE 830

FIRST RELEASE - DRN 00081

		DISTRIBUTION	
		FILE	QTY
881501-231	DA 1410		
NEXT ASSY	USED ON		
APPLICATION			

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PROJECT NO.	
DATE	11-15-67
DRAWN	Duckworth
CHECKED	
APPROVED	
SCALE	

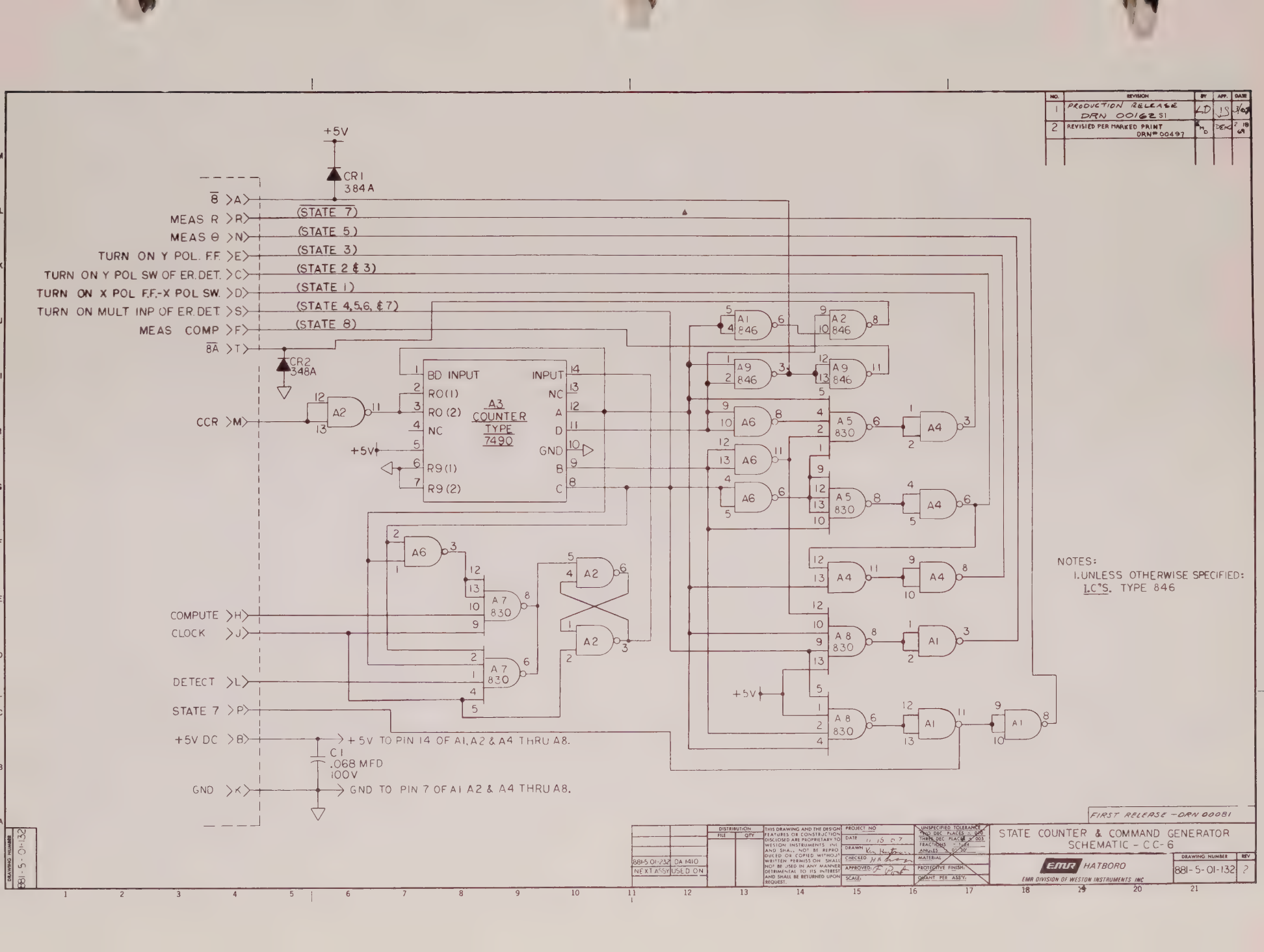
UNSPECIFIED TOLERANCE
TWO DEC. PLACES ± .010
THREE DEC. PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0° 30'
MATERIAL
PROTECTIVE FINISH
QUANT PER ASSY.

SYNCHRONOUS CIRCUIT - CC2 SCHEMATIC

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

DRAWING NUMBER 881-5-01-131 REV. 1

DRAWING NUMBER 881-5-01-131



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   I.C.'S. TYPE 846

NO.	REVISION	BY	APP.	DATE
1	PRODUCTION RELEASE DRN 00162 S1	KD	JS	1/69
2	REVISED PER MARKED PRINT DRN# 00497	[illegible]	DEMO	2 IB 69

FIRST RELEASE - DRN 00081

DRAWING NUMBER 881-5-01-132

DISTRIBUTION: FILE QTY

881-5-01-232 DA 1410

NEXT ASSY USED ON

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PROJECT NO

DATE 1-15-67

DRAWN Ken Hutton

CHECKED N/A

APPROVED:

SCALE:

UNSPECIFIED TOLERANCE
TWO DEC PLACES ± .01
THREE DEC PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'

MATERIAL

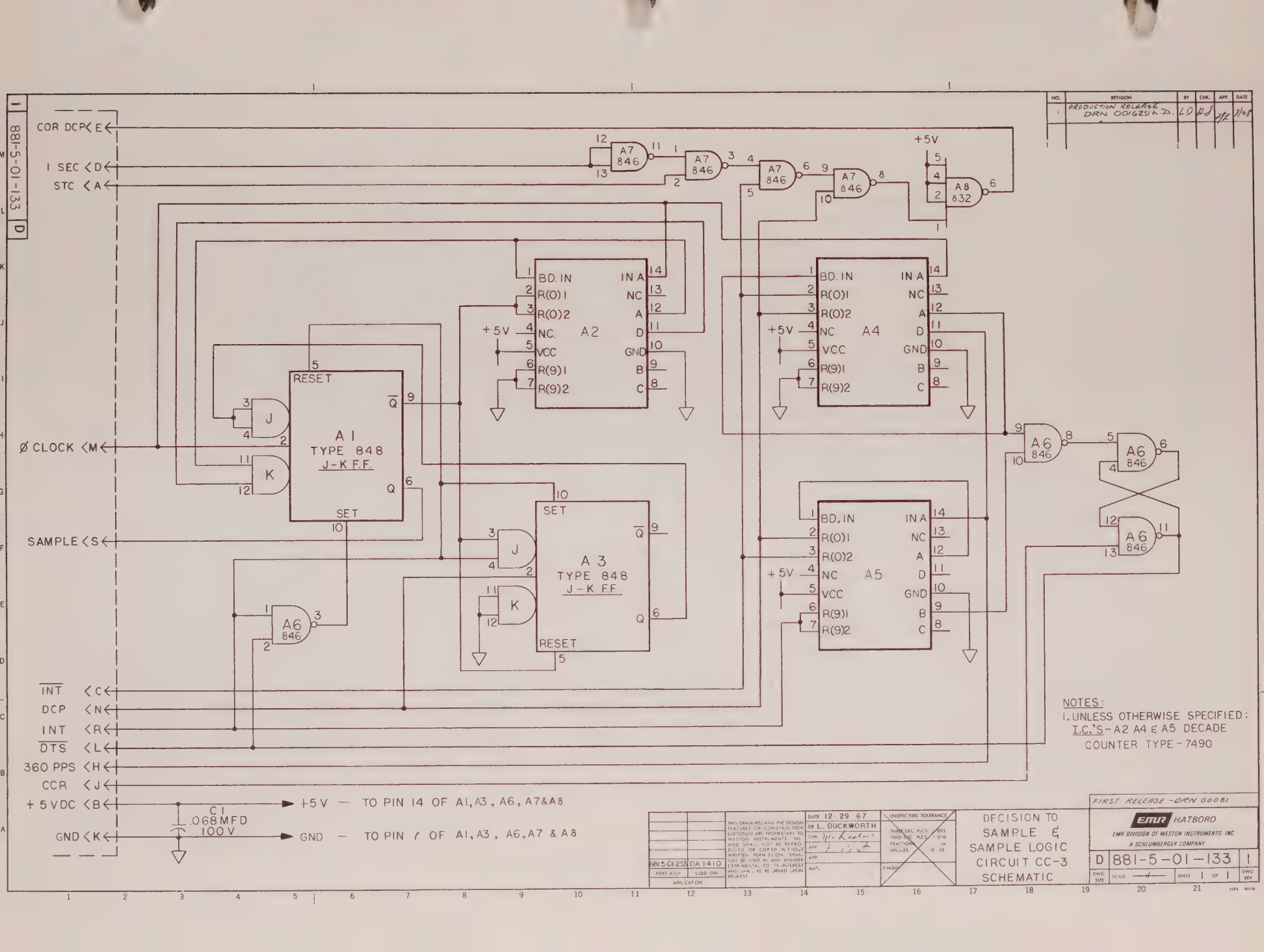
PROTECTIVE FINISH:

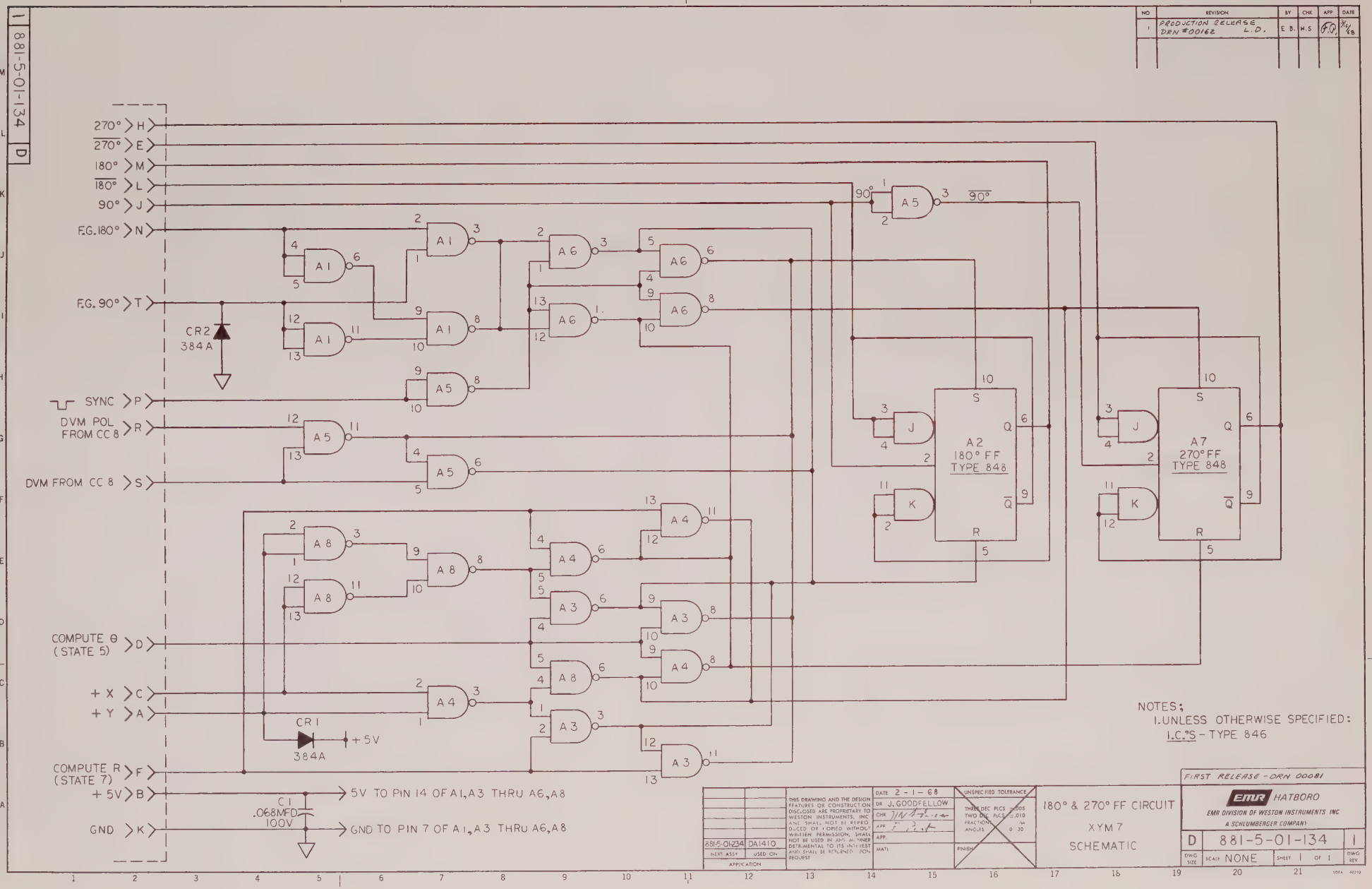
QUANT PER ASSY:

STATE COUNTER & COMMAND GENERATOR SCHEMATIC - CC-6

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC

DRAWING NUMBER 881-5-01-132 REV ?


881-5-01-133 D
COR DCP E
1 SEC D
STC A
Ø CLOCK M
SAMPLE S
INT C
DCP N
INT R
DTS L
360 PPS H
CCR J
+5VDC B
GND K
C1
.068MFD
100V
+5V — TO PIN 14 OF A1, A3, A6, A7&A8
GND — TO PIN 7 OF A1, A3, A6, A7 & A8
A1
TYPE 848
J-K F.F.
A2
A3
TYPE 848
J-K F.F
A4
A5
DECADE COUNTER TYPE-7490
A7 846
A8 832
A6 846
BD. IN
R(0)1
R(0)2
NC.
VCC
R(9)1
R(9)2
IN A
NC
A
D
GND
B
C
RESET
SET
J
K
Q
+5V
NO. REVISION BY CHK. APP. DATE
1 PRODUCTION RELEASE DRN 00162SIR.D. LD
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
I.C.'S - A2 A4 & A5 DECADE
COUNTER TYPE - 7490
DECISION TO SAMPLE & SAMPLE LOGIC CIRCUIT CC-3 SCHEMATIC
FIRST RELEASE - DRN 00081
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
D 881-5-01-133 1
DR L. DUCKWORTH
DATE 12-29-67
APP. CAT ON
NEXT ASSY USED ON


881-5-01-134 D
270° H
270° E
180° M
180° L
90° J
F.G. 180° N
F.G. 90° T
CR2 384A
SYNC P
DVM POL FROM CC 8 R
DVM FROM CC 8 S
COMPUTE θ (STATE 5) D
+ X C
+ Y A
CR1 384A
+5V
COMPUTE R (STATE 7) F
+5V B
GND K
C1 .068MFD 100V
5V TO PIN 14 OF A1, A3 THRU A6, A8
GND TO PIN 7 OF A1, A3 THRU A6, A8
A1
A2 180° FF TYPE 848
A3
A4
A5
A6
A7 270° FF TYPE 848
A8
J
K
S
R
Q
90°
NOTES;
1. UNLESS OTHERWISE SPECIFIED:
I.C.'S - TYPE 846
NO 1 REVISION: PRODUCTION RELEASE DRN #00162 L.D. BY E.B. CHK W.S APP F.D. DATE 3/4/68
FIRST RELEASE - DRN 00081
180° & 270° FF CIRCUIT
XYM 7
SCHEMATIC
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
D 881-5-01-134 1
SCALE NONE SHEET 1 OF 1
DATE 2-1-68 DR J. GOODFELLOW
UNSPECIFIED TOLERANCE
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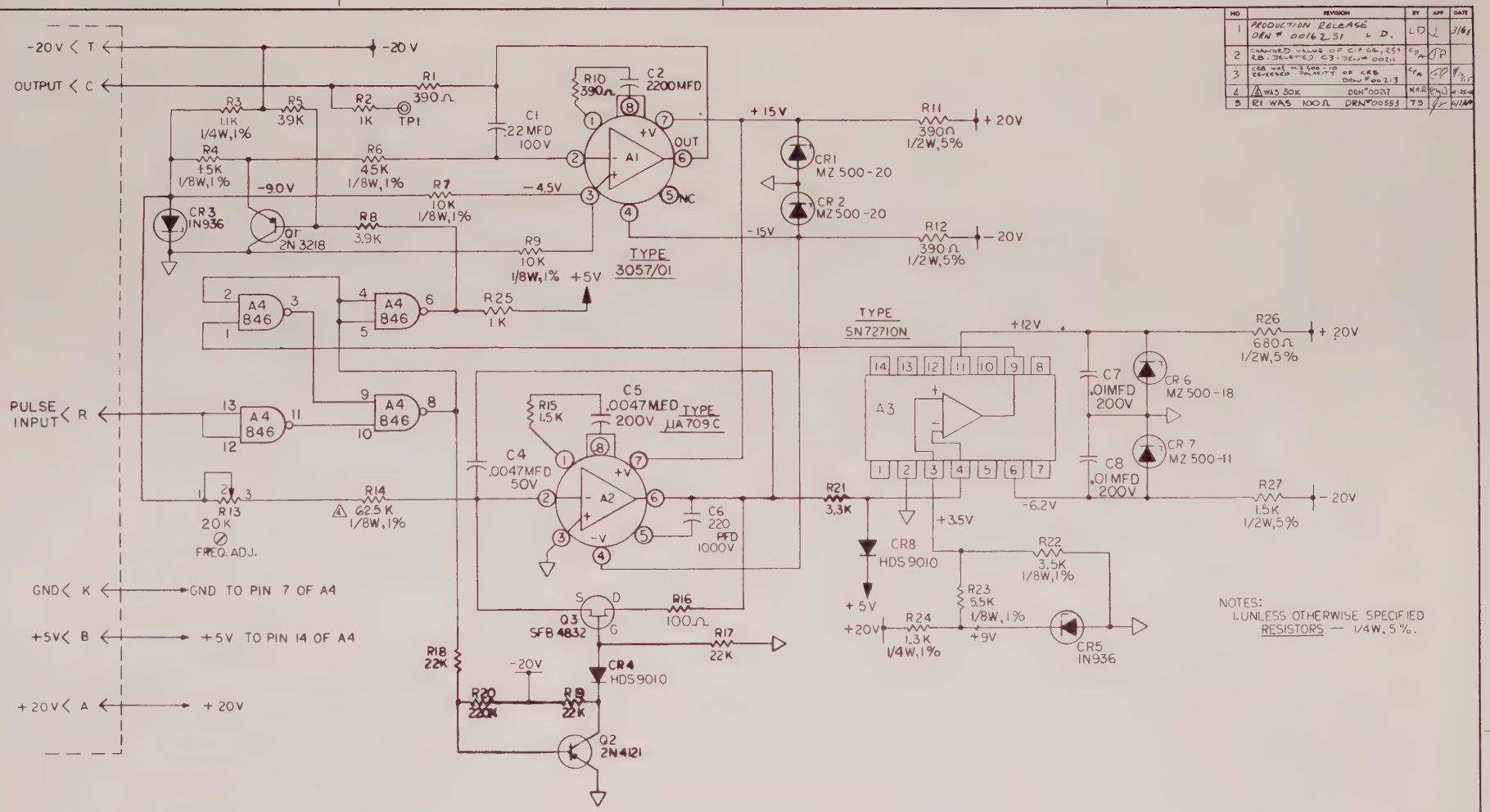
881-5-01-134 DA1410
NEXT ASSY USED ON
APPLICATION



NO	REVISION	BY	APP	DATE
1	PRODUCTION RELEASE DRN # 00162 SI L D.	LD	L	3/64
2	CHANGED VALUE OF C1 FR 22μ TO 25μ RB. DELETED C3. DRN # 00211	CP	CP	
3	CRB WAS MISSING TO REFERENCE POLARITY OF CR8 DRN # 00213	CP	CP	11/15
4	⚠ WAS 50K DRN # 00217	KHA	CHO	4-25-65
5	R1 WAS 100Ω DRN # 00553	TS		6/1/65

FIRST RELEASE - DRN 00081

DISTRIBUTION	FILE	QTY
88-5-01-235	DA 1410	

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PROJECT NO
DATE 1-12-67
DRAWN: Ken Hatboro
CHECKED: HA
APPROVED: F Cook
SCALE:

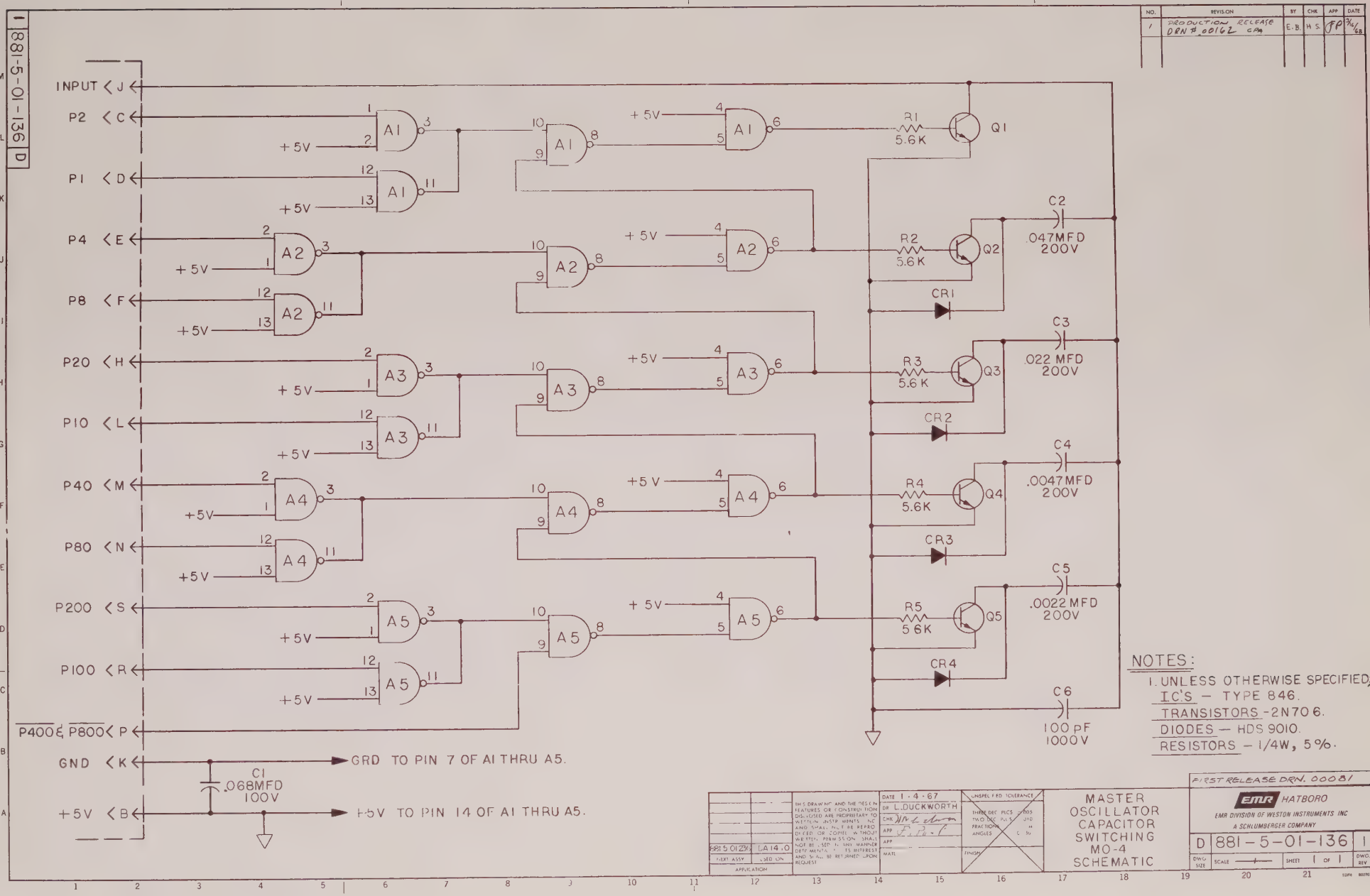
UNSPECIFIED TOLERANCE
TWO DEC PLACES ± .015
THREE DEC PLACES ± .003
FRACTIONS ± 1/64
ANGLES ± 0°30'
MATERIAL
PROTECTIVE FINISH
PRINT PER ASSY.

MASTER OSCILLATOR CONTROL CIRCUITS NO-1 SCHEMATIC

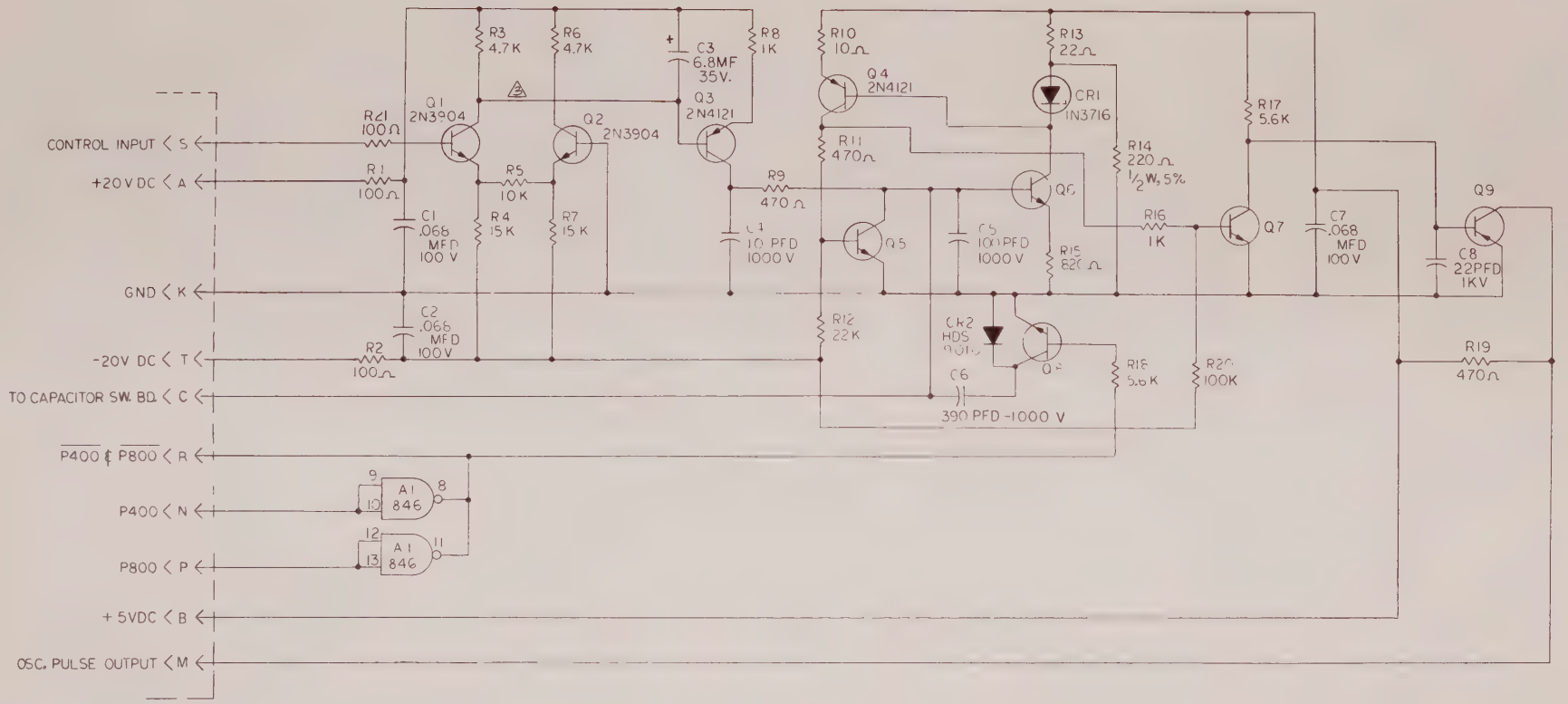
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC

DRAWING NUMBER 681-5-01-135 REV 5

DRAWING NUMBER 1-5-01-135


881-5-01-136 D
NO. REVISION BY CHK APP DATE
1 PRODUCTION RELEASE DRN # 00162 CPR E.B. H.S. JP 7/1/68
INPUT J
P2 C
P1 D
P4 E
P8 F
P20 H
P10 L
P40 M
P80 N
P200 S
P100 R
P400 & P800 P
GND K
+5V B
+5V
A1
A2
A3
A4
A5
R1 5.6K
R2 5.6K
R3 5.6 K
R4 5.6K
R5 5.6K
Q1
Q2
Q3
Q4
Q5
CR1
CR2
CR3
CR4
C1 .068MFD 100V
C2 .047MFD 200V
C3 .022 MFD 200V
C4 .0047MFD 200V
C5 .0022 MFD 200V
C6 100 pF 1000V
GRD TO PIN 7 OF A1 THRU A5.
+5V TO PIN 14 OF A1 THRU A5.
NOTES:
1. UNLESS OTHERWISE SPECIFIED,
IC'S — TYPE 846.
TRANSISTORS - 2N706.
DIODES — HDS 9010.
RESISTORS — 1/4W, 5%.
DATE 1-4-67
DR L.DUCKWORTH
CHK
APP
APP
MATL
UNSPECIFIED TOLERANCE
THREE DEC PLCS ±.005
TWO DEC PLCS ±.010
FRACTIONS ±
ANGLES ±
FINISH
MASTER OSCILLATOR CAPACITOR SWITCHING MO-4 SCHEMATIC
FIRST RELEASE DRN. 00081
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
D 881-5-01-136 1
DWG SIZE SCALE SHEET 1 OF 1 DWG REV

NO.	REVISION	BY	APP.	DATE
1	PRODUCTION RELEASE DRN 00131			
2	C3 WAS .01MF 600V DRN 00283			
3	REMOVED J1, ADDED R21 C8 WAS 100 PFD DRN 00312	TS		



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
RESISTORS - 1/4W, 5%
TRANSISTORS - 2N706

FIRST RELEASE - DRN 00128

DRAWING NUMBER 6M1-5-01-137

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PROJECT NO.:
DATE 6DEC67
DRAWN
CHECKED
APPROVED
SCALE:

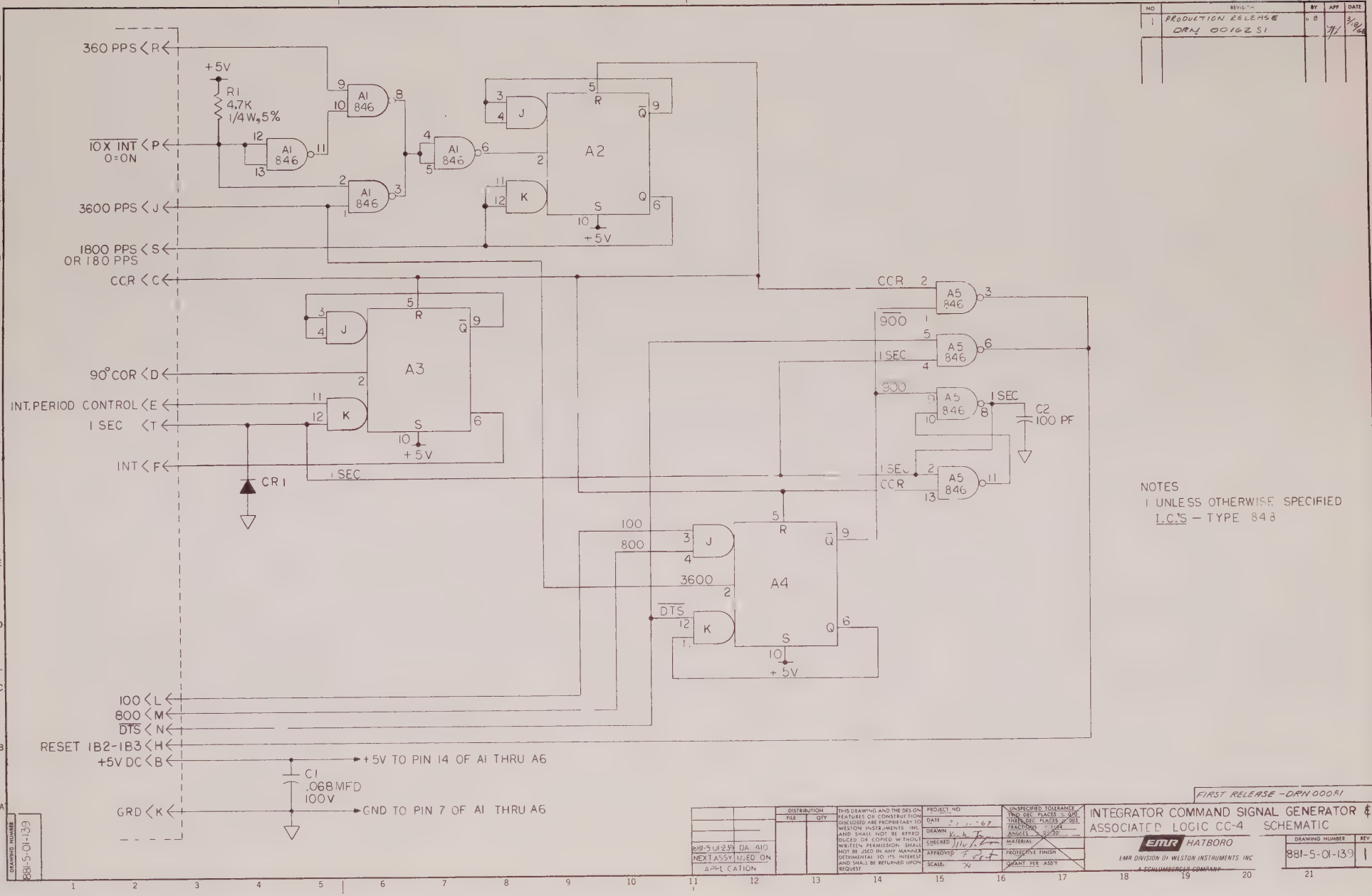
UNSPECIFIED TOLERANCE
TWO DEC. PLACES ± .005
THREE DEC. PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0°30'
MATERIAL
PROTECTIVE FINISH
QUANT. PER ASS'Y.

VARIABLE FREQ. PULSE GENERATOR M05
SCHEMATIC

EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
HATBORO

DRAWING NUMBER 6M1-5-01-137 REV 3

SEE 1-237 01 1410
NEXT ASSY USED ON
APPLICATION



NO	REVISION	BY	APP	DATE
1	PRODUCTION RELEASE DRN 0016251	W B		3/19/68

NOTES
1 UNLESS OTHERWISE SPECIFIED
I.C.'S – TYPE 848

FIRST RELEASE – DRN 000R1

DRAWING NUMBER 881-5-01-139

881-5-01-239 DA 410
NEXT ASSY USED ON
APPLICATION

DISTRIBUTION: FILE | QTY

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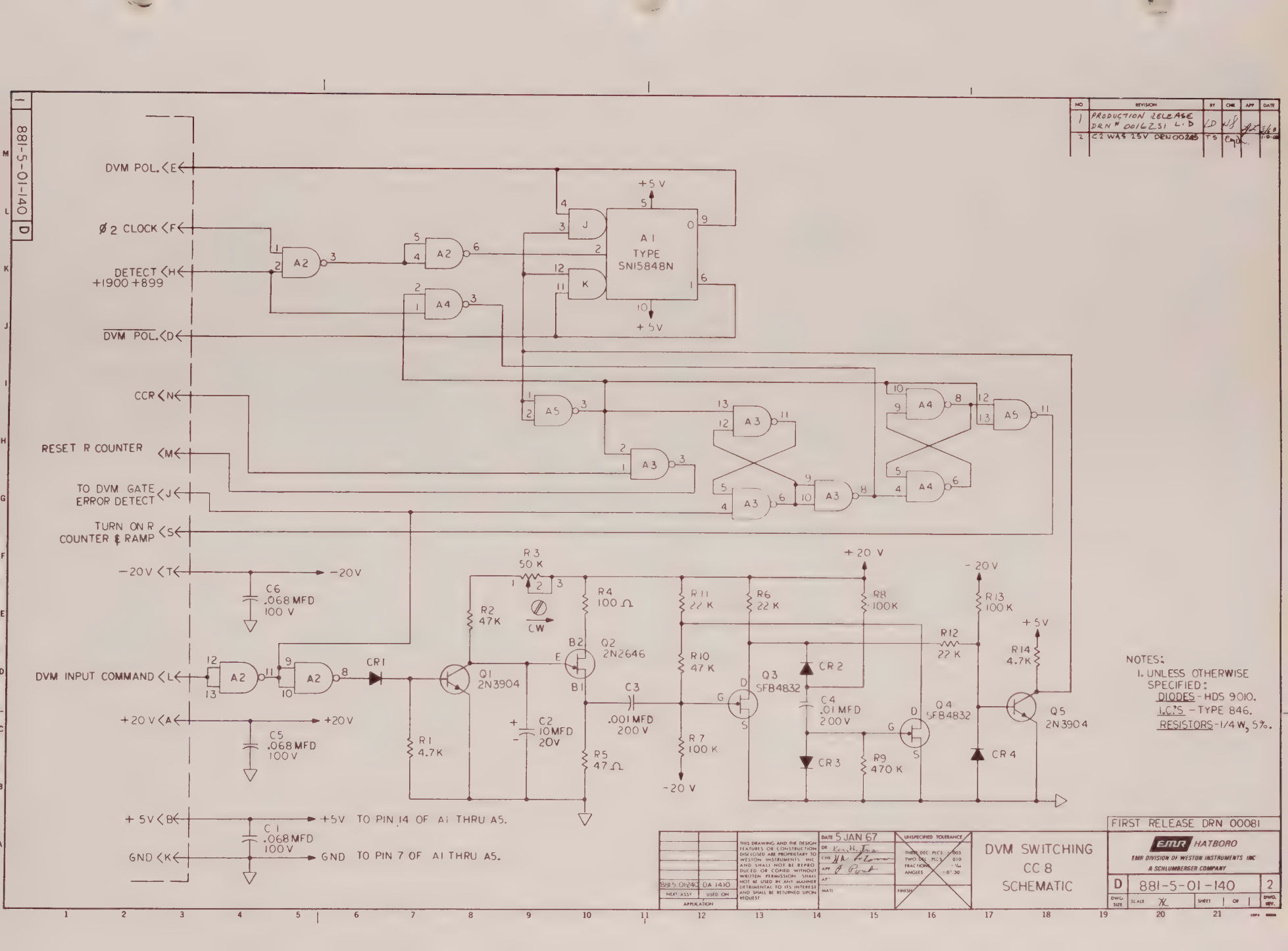
PROJECT NO
DATE 7-11-67
DRAWN
CHECKED
APPROVED
SCALE: NONE

UNSPECIFIED TOLERANCE
TWO DEC PLACES ± .010
THREE DEC PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0° 30'
MATERIAL
PROTECTIVE FINISH
QUANT PER ASSY

INTEGRATOR COMMAND SIGNAL GENERATOR & ASSOCIATED LOGIC CC-4 SCHEMATIC

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

DRAWING NUMBER 881-5-01-139 REV 1



NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE DRN # 00162S1 L.D	VD	KS		5/6/68
2	C2 WAS 25V DRN 00245	TS			11-8-68

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
DIODES - HDS 9010.
I.C.'S - TYPE 846.
RESISTORS - 1/4 W, 5%.

DATE	5 JAN 67	UNSPECIFIED TOLERANCE	
DR	Ken H. Fox	THREE DEC PLCS	.005
CHK	Wm Palmer	TWO DEC PLCS	.010
APP	J Grant	FRACTIONS	1/64
AF		ANGLES	±0° 30'
MATL		FINISH	

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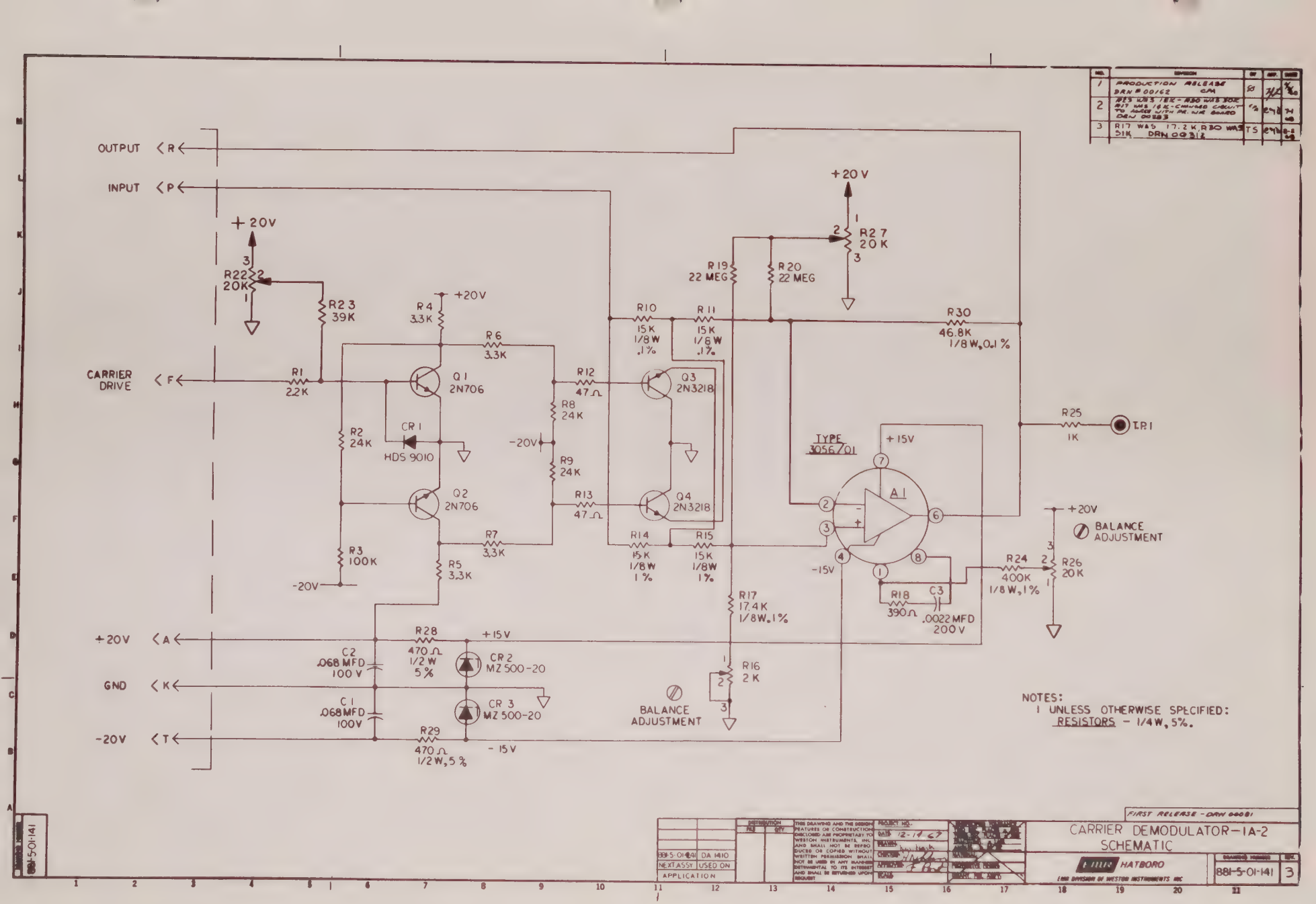
881-5-01-240 DA 1410
NEXT ASSY | USED ON
APPLICATION

DVM SWITCHING
CC 8
SCHEMATIC

FIRST RELEASE DRN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D	881-5-01-140	2
DWG SIZE	SCALE X	SHEET 1 OF 1



NOTES:
1 UNLESS OTHERWISE SPECIFIED:
RESISTORS - 1/4W, 5%.

NO.	REVISION	BY	DATE	APPD
1	PRODUCTION RELEASE DRN # 00162 CM	RS	7/1/67	
2	R23 WAS 18K - R30 WAS 50K R17 WAS 16K - CHANGED CIRCUIT TO AGREE WITH PC. W.A. BOARD DRN 00283	TS	8/4/67	
3	R17 WAS 17.2K, R30 WAS 51K DRN 00318	TS	8/4/67	

FIRST RELEASE - DRN 00081

CARRIER DEMODULATOR-1A-2 SCHEMATIC

HATBORO — LFE DIVISION OF WESTON INSTRUMENTS INC

DRAWING NUMBER 881-5-01-141 REV. 3

881-5-01-141

DISTRIBUTION REQ QTY

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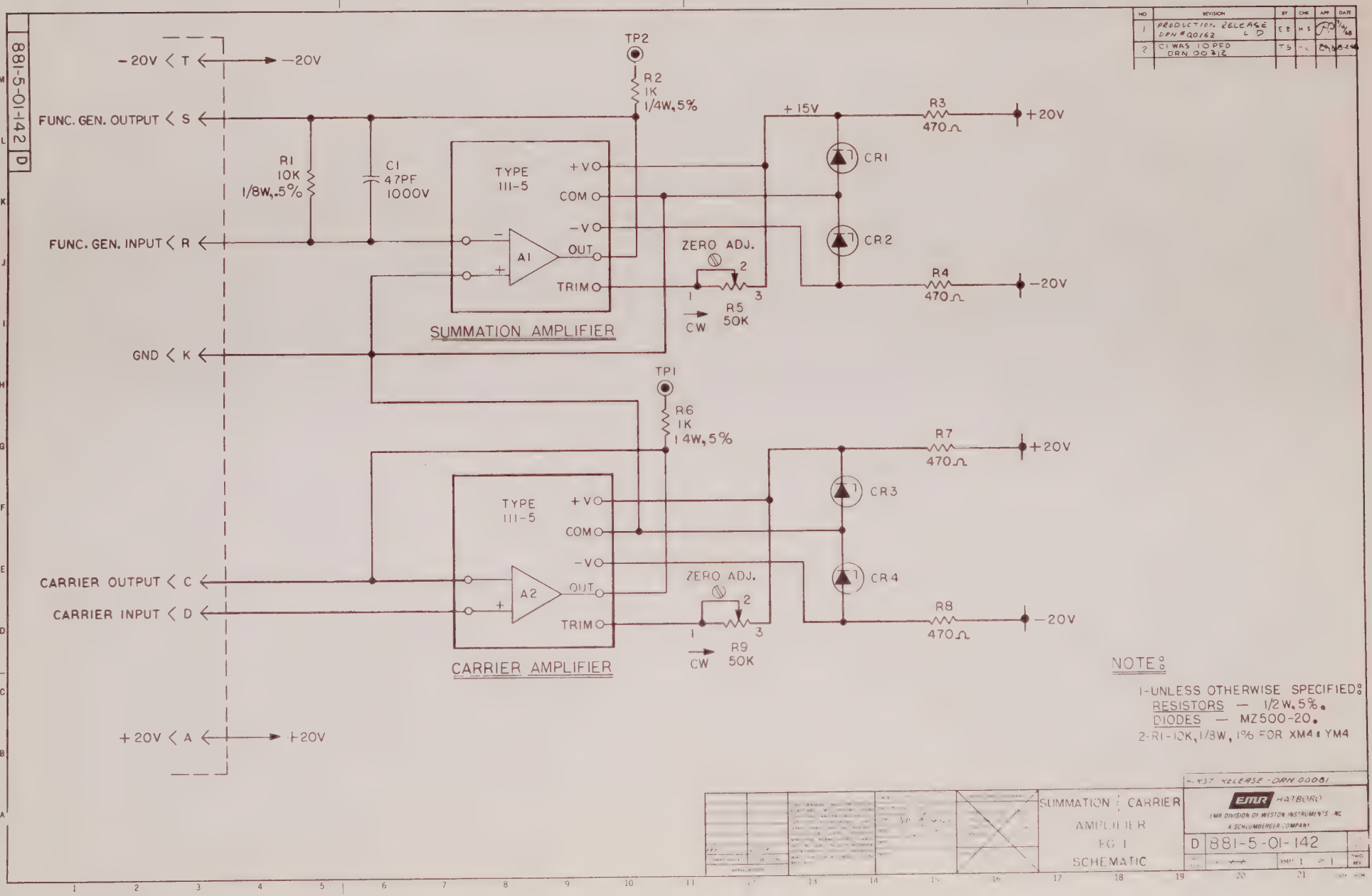
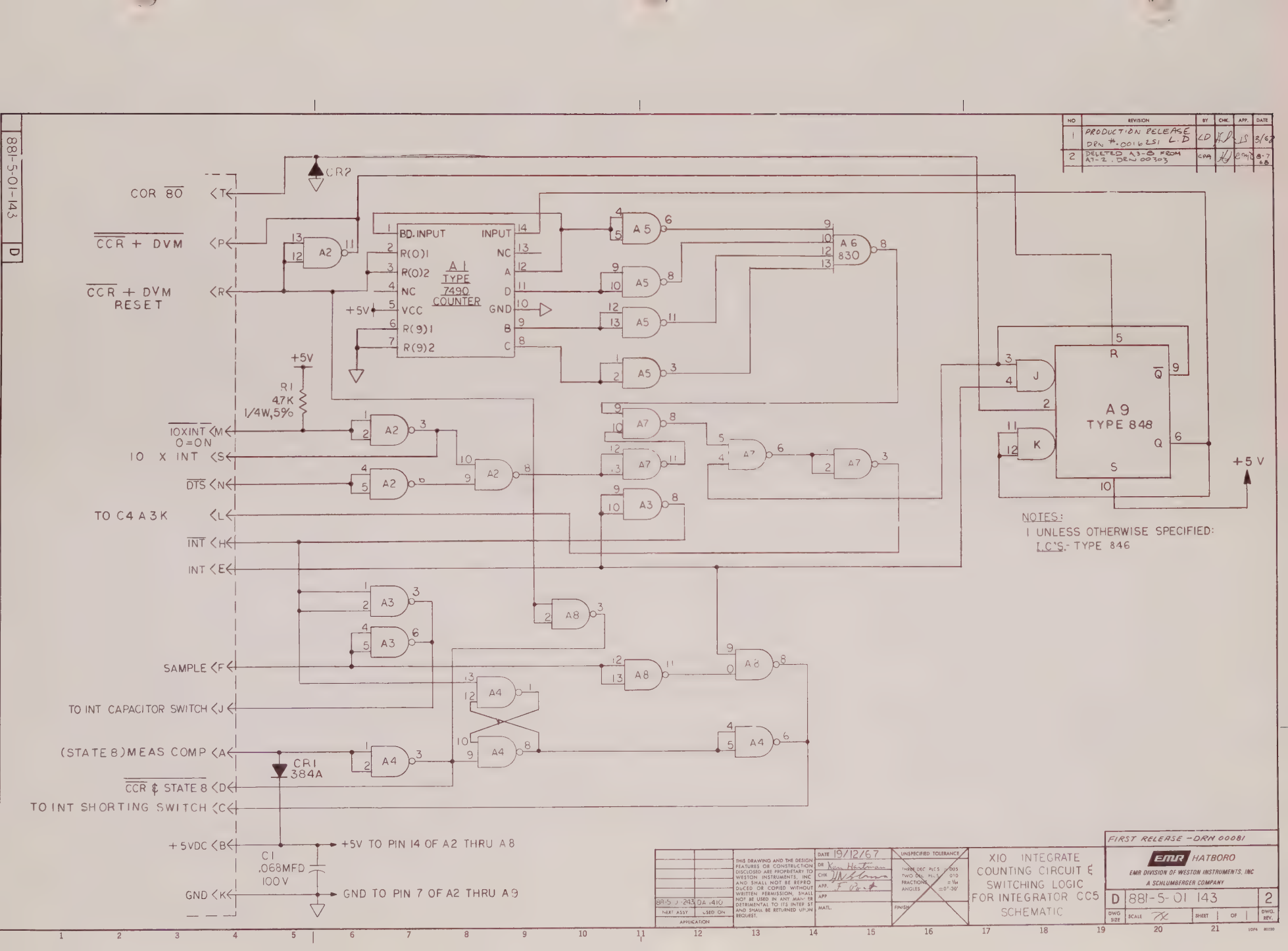
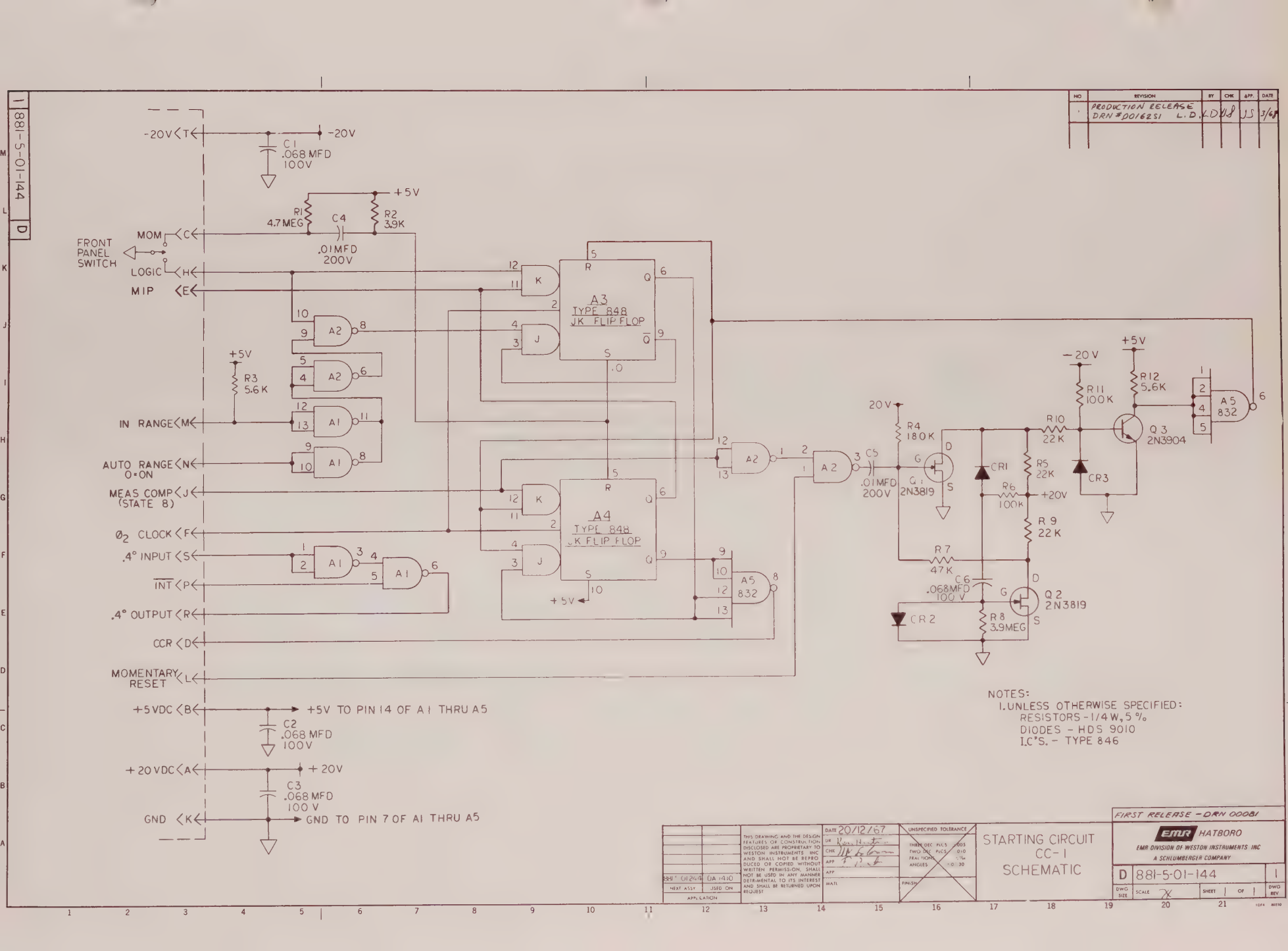
PROJECT NO.
DATE 12-19-67
DRAWN
CHECKED
APPROVED
SCALE

881-5-01-141 DA 1410
NEXT ASSY USED ON
APPLICATION


881-5-01-142 D
-20V T
-20V
FUNC. GEN. OUTPUT S
FUNC. GEN. INPUT R
GND K
+20V A
+20V
TP2
R2
1K
1/4W,5%
R1
10K
1/8W,.5%
C1
47PF
1000V
TYPE
111-5
+VO
COM
-VO
OUT
TRIM
A1
SUMMATION AMPLIFIER
+15V
R3
470Ω
+20V
CR1
CR2
ZERO ADJ.
R4
470Ω
-20V
R5
50K
CW
TP1
R6
1K
1/4W,5%
R7
470Ω
+20V
CR3
CR4
CARRIER OUTPUT C
CARRIER INPUT D
A2
CARRIER AMPLIFIER
R8
470Ω
-20V
R9
50K
CW
NOTE:
1-UNLESS OTHERWISE SPECIFIED:
RESISTORS — 1/2W,5%.
DIODES — MZ500-20.
2-R1-10K,1/8W,1% FOR XM4 & YM4
REVISION
PRODUCTION RELEASE DRN #00162
CI WAS 10PFD DRN 00312
SUMMATION / CARRIER AMPLIFIER
FG 1
SCHEMATIC
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY
D 881-5-01-142


881-5-01-143 D
NO | REVISION | BY | CHK. | APP. | DATE
1 | PRODUCTION RELEASE DRN #.00162SI L.D | LD | | | 3/62
2 | DELETED A3-8 FROM A7-2. DRN 00303 | CPA | | | 8-7-68
COR 80
CCR + DVM
CCR + DVM RESET
TO C4 A3K
SAMPLE
TO INT CAPACITOR SWITCH
(STATE 8) MEAS COMP
CCR & STATE 8
TO INT SHORTING SWITCH
+5VDC
GND
CR2
CR1 384A
R1 4.7K 1/4W,5%
C1 .068MFD 100V
+5V TO PIN 14 OF A2 THRU A8
GND TO PIN 7 OF A2 THRU A9
A1 TYPE 7490 COUNTER
BD. INPUT
INPUT
R(0)1
R(0)2
NC
VCC
R(9)1
R(9)2
A
D
GND
B
C
A9 TYPE 848
A6 830
+5V
NOTES:
1 UNLESS OTHERWISE SPECIFIED:
I.C'S.- TYPE 846
FIRST RELEASE - DRN 00081
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY
X10 INTEGRATE COUNTING CIRCUIT & SWITCHING LOGIC FOR INTEGRATOR CC5 SCHEMATIC
D 881-5-01 143 2



NO	REVISION	BY	CHK	APP.	DATE
1	PRODUCTION RELEASE DRN #D016251 L.D.	LD	DB	JJ	3/67

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   RESISTORS - 1/4 W, 5 %
   DIODES - HDS 9010
   I.C'S. - TYPE 846

FIRST RELEASE - DRN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

STARTING CIRCUIT
CC-1
SCHEMATIC

D | 881-5-01-144 | 1

DWG SIZE D | SCALE 2X | SHEET 1 OF 1 | DWG REV 1

DATE 20/12/67

UNSPECIFIED TOLERANCE
THREE DEC PLCS ±.005
TWO DEC PLCS ±.010
FRACTIONS ±1/64
ANGLES ±0°30'

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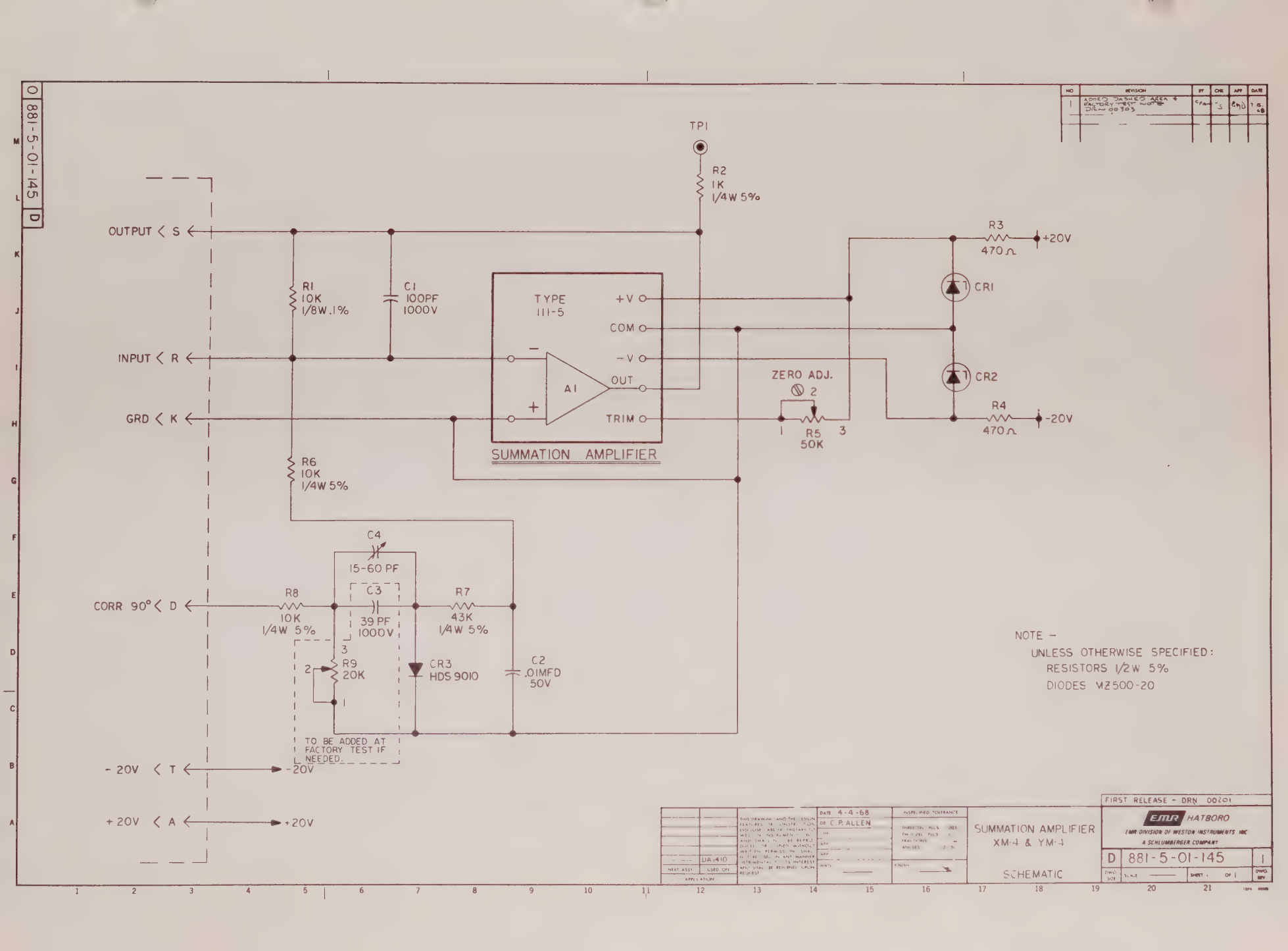
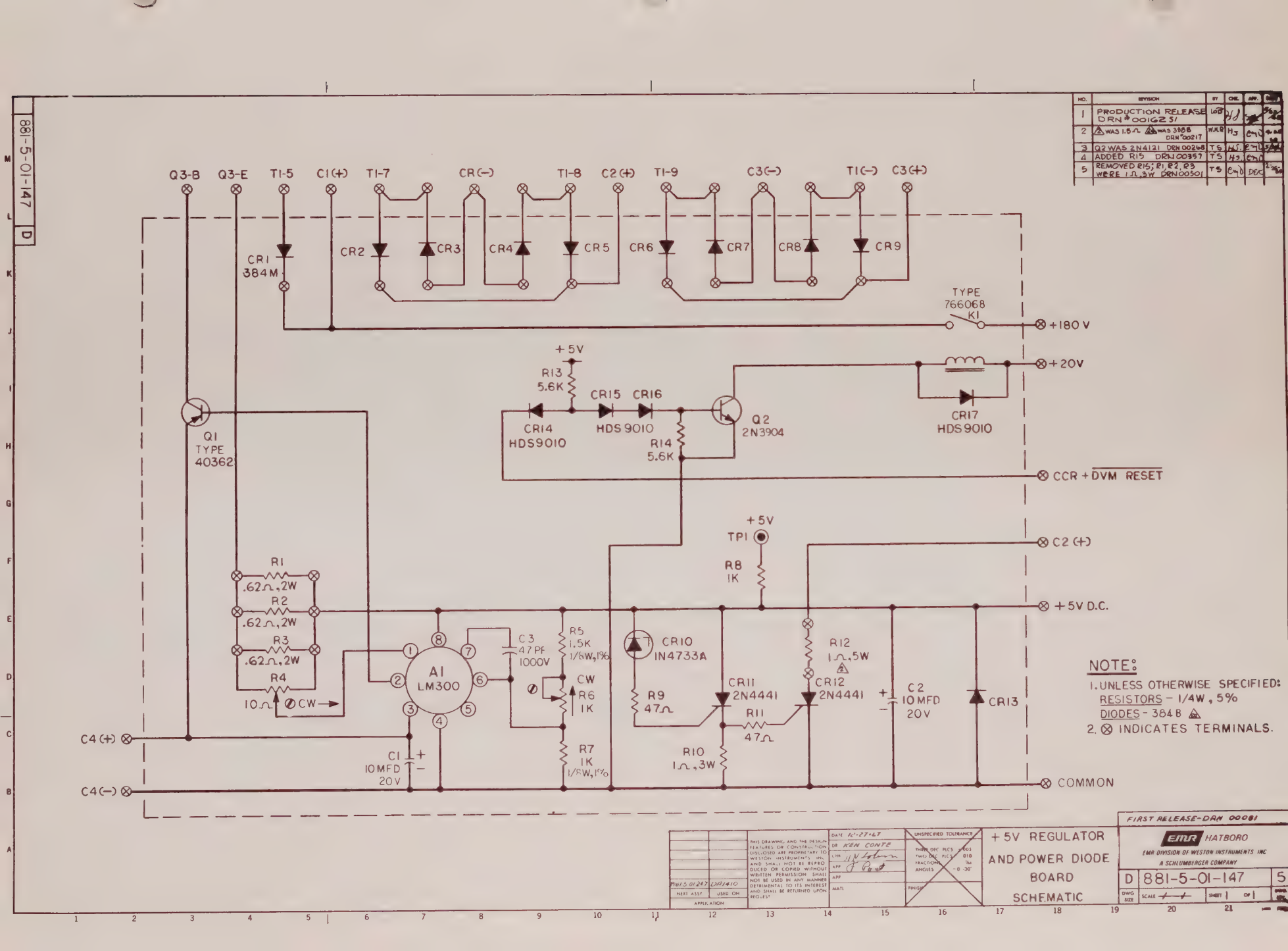
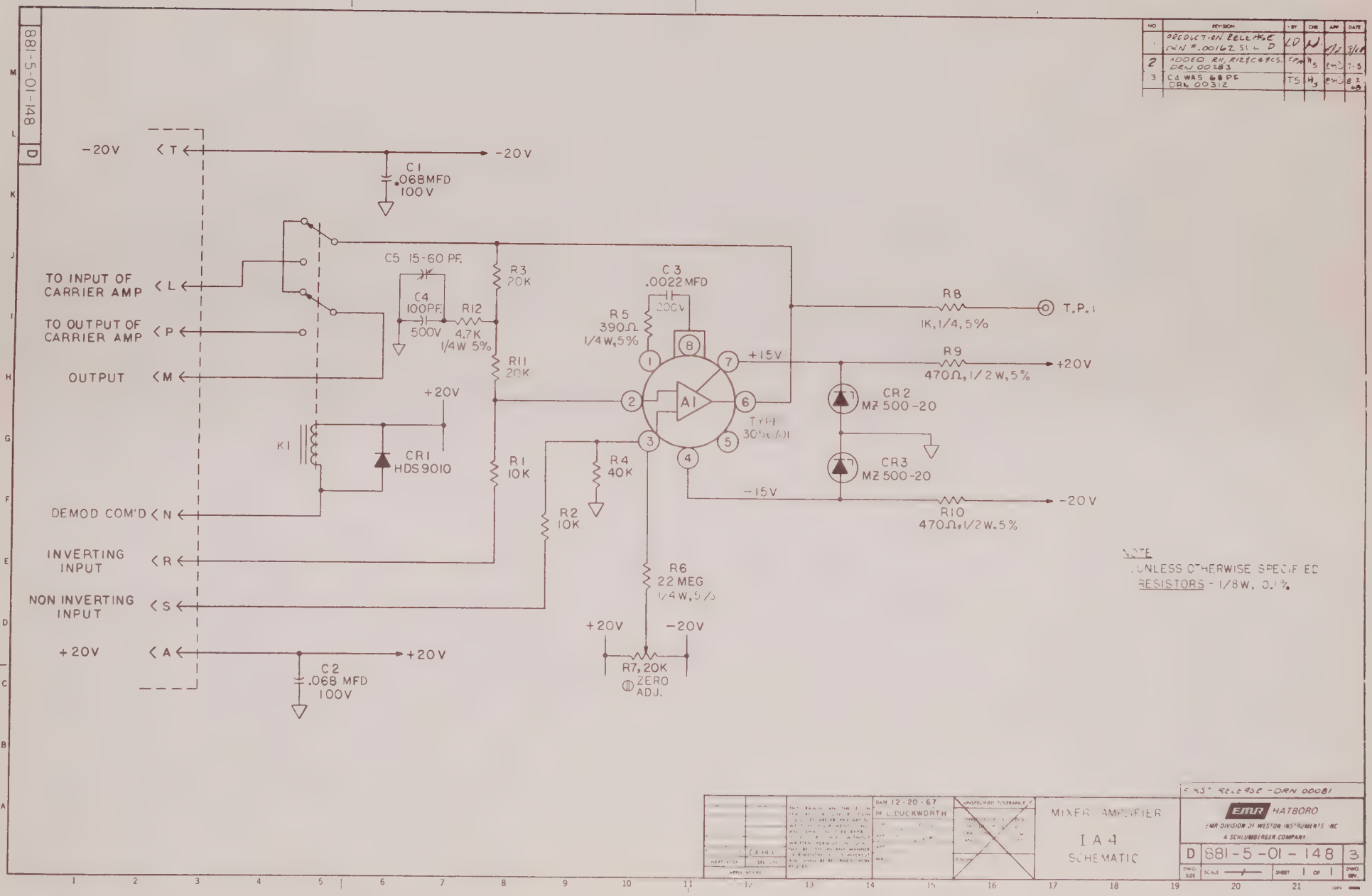
881 01244 0A 1410
NEXT ASSY | USED ON
APPLICATION

FINISH
MATL


TP1
R2
1K
1/4W 5%
OUTPUT < S
INPUT < R
GRD < K
R1
10K
1/8W 1%
C1
100PF
1000V
TYPE
111-5
+V
COM
-V
OUT
TRIM
A1
SUMMATION AMPLIFIER
R3
470Ω
+20V
CR1
CR2
ZERO ADJ.
2
1
R5
50K
3
R4
470Ω
-20V
R6
10K
1/4W 5%
C4
15-60 PF
CORR 90° < D
R8
10K
1/4W 5%
C3
39 PF
1000V
R7
43K
1/4W 5%
3
2
R9
20K
1
CR3
HDS 9010
C2
.01MFD
50V
TO BE ADDED AT
FACTORY TEST IF
NEEDED.
- 20V < T
-20V
+ 20V < A
+20V
NOTE -
UNLESS OTHERWISE SPECIFIED:
RESISTORS 1/2W 5%
DIODES MZ500-20
REVISION
1
ADDED DASHED AREA & FACTORY TEST NOTE DRN 00303
FIRST RELEASE - DRN 00201
DATE 4-4-68
DR C.P. ALLEN
SUMMATION AMPLIFIER
XM-4 & YM-4
SCHEMATIC
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
D 881-5-01-145 1
0 881-5-01-145 D


881-5-01-147 D
Q3-B
Q3-E
TI-5
C1(+)
TI-7
CR(-)
TI-8
C2(+)
TI-9
C3(-)
TI(-)
C3(+)
CR1 384M
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
TYPE 766068 K1
+180 V
+20V
+5V
R13 5.6K
CR15
CR16
CR14 HDS9010
HDS 9010
R14 5.6K
Q2 2N3904
CR17 HDS9010
Q1 TYPE 40362
CCR + DVM RESET
+5V
TP1
C2 (+)
R8 1K
R1 .62Ω, 2W
R2 .62Ω, 2W
R3 .62Ω, 2W
R4 10Ω CW
+5V D.C.
A1 LM300
C3 47 PF 1000V
R5 1.5K 1/8W, 1%
CW R6 1K
R7 1K 1/8W, 1%
CR10 IN4733A
R9 47Ω
CR11 2N4441
R10 1Ω, 3W
R11 47Ω
R12 1Ω, 5W
CR12 2N4441
C2 10 MFD 20V
CR13
C4 (+)
C4 (-)
C1 10 MFD 20V
COMMON
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
RESISTORS - 1/4W, 5%
DIODES - 3848
2. ⊗ INDICATES TERMINALS.
NO. REVISION BY CHK APP DATE
1 PRODUCTION RELEASE DRN # 001625 LGB
2 WAS 1.5Ω WAS 3888 DRN 00217 W.K.B HJ
3 Q2 WAS 2N4121 DRN 00268 TS HJ
4 ADDED R15 DRN 00357 TS HJ
5 REMOVED R15; R1, R2, R3 WERE 1Ω, 3W DRN 00501 TS
FIRST RELEASE-DRN 00081
+5V REGULATOR AND POWER DIODE BOARD SCHEMATIC
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
D 881-5-01-147 5
SHEET 1 OF 1



NO	REVISION	BY	CHK	APP	DATE
	PRODUCTION RELEASE DRN # 00162 SH 1 D	LD	W		3/68
2	ADDED R11,R12,C4,C5. DRN 00283	EPM	HS	EMS	7-5
3	C4 WAS 68 PF DRN 00312	TS	HS	EMS	8 2 68

NOTE
UNLESS OTHERWISE SPECIFIED
RESISTORS - 1/8W, 0.1%

FIRST RELEASE - DRN 00081

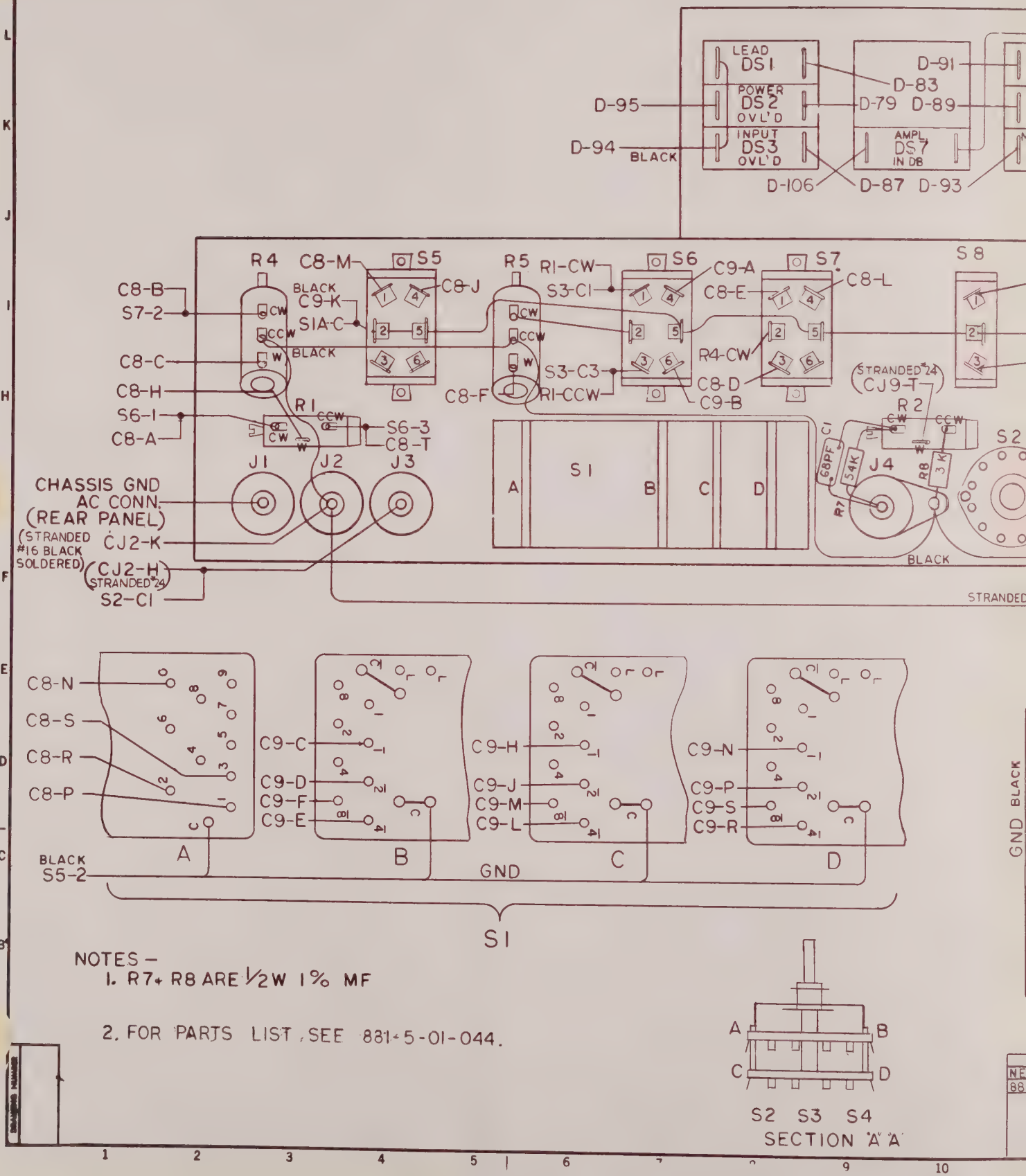
DATE 12-20-67
DR L.DUCKWORTH

MIXER AMPLIFIER
IA4
SCHEMATIC

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D 881-5-01-148 3

DWG SIZE | SCALE | SHEET 1 OF 1 | DWG REV.



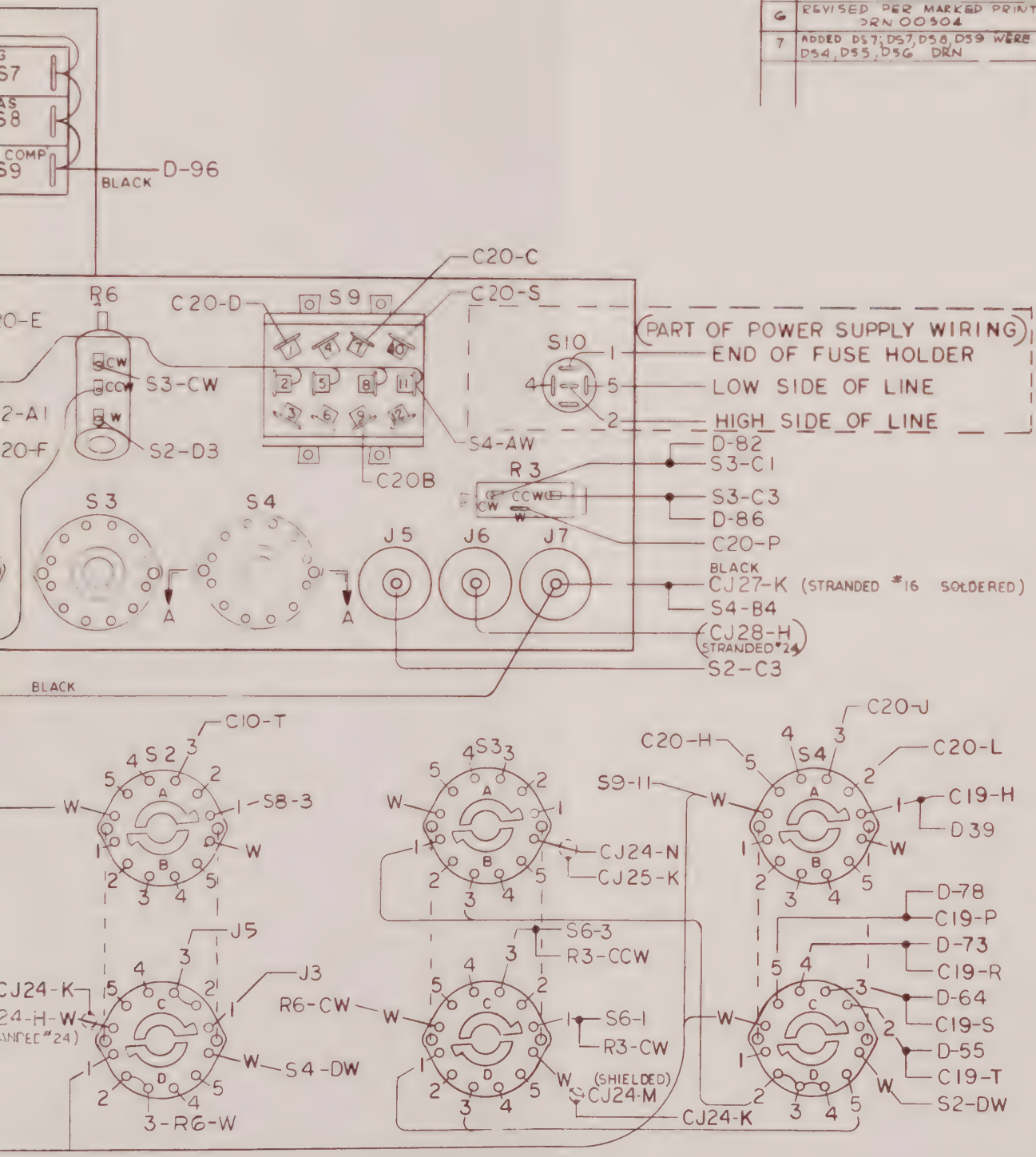
NOTES –

1. R7 + R8 ARE ½W 1% MF

2. FOR PARTS LIST, SEE 881-5-01-044.

S2 S3 S4
SECTION "A" "A"

NO.	REVISION	BY	APP.	DATE
1	REVISED PER MARKED PRINT DRN* 00161	EW	FP	3-3
2	ADDED CAPACITOR C1 DRN 00303	CPA		7-16
3	R8 WAS 4.7K DRN 00352	HS		
4	REVISED WIRING PER MARKED PRINT- DRN 00344			
5	ADDED JPR FROM S3-C2 TO S3-D2 ADDED JPR FROM S3-DW TO S4-B5 REMOVED R8 FROM S10 DRN 00401	TS		
6	REVISED PER MARKED PRINT DRN 00504	TS		3-12
7	ADDED DS7, DS7, DS8, DS9 WERE DS4, DS5, DS6 DRN	END		3-12-69



FIRST RELEASE DRN* 00138

12	13	14	15	16	17	18	19	20	21		

LICATION
SSY | USED ON
044 | 1410

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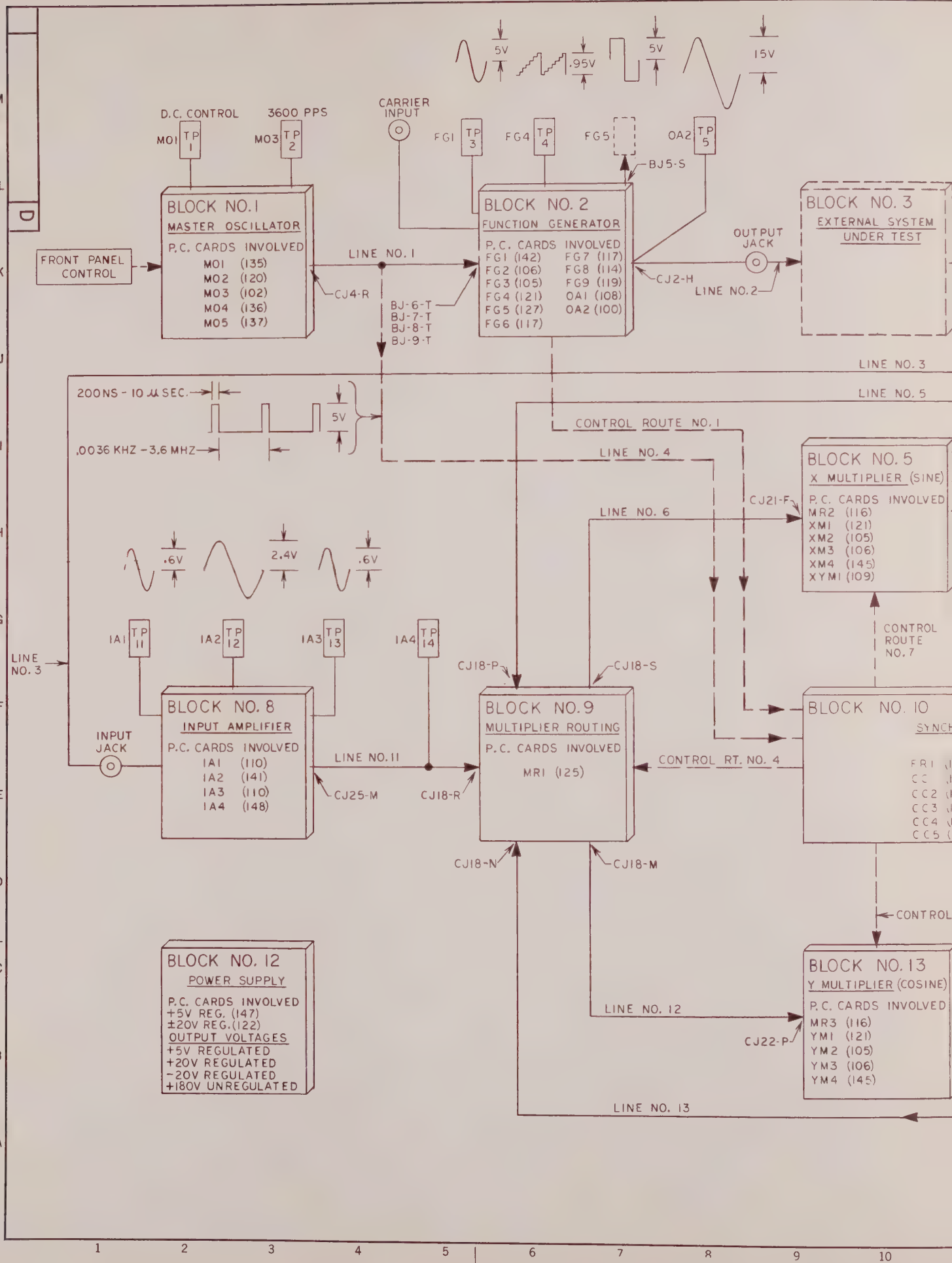
PROJECT NO.:
DATE: FEB. 26 1968
DRAWN: W. BRICKS
CHECKED:
APPROVED: F. Root
SCALE:

UNSPECIFIED TOLERANCE
TWO DEC. PLACES ± .010
THREE DEC. PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0° 30'
MATERIAL:
PROTECTIVE FINISH:
QUANT. PER. ASSY:

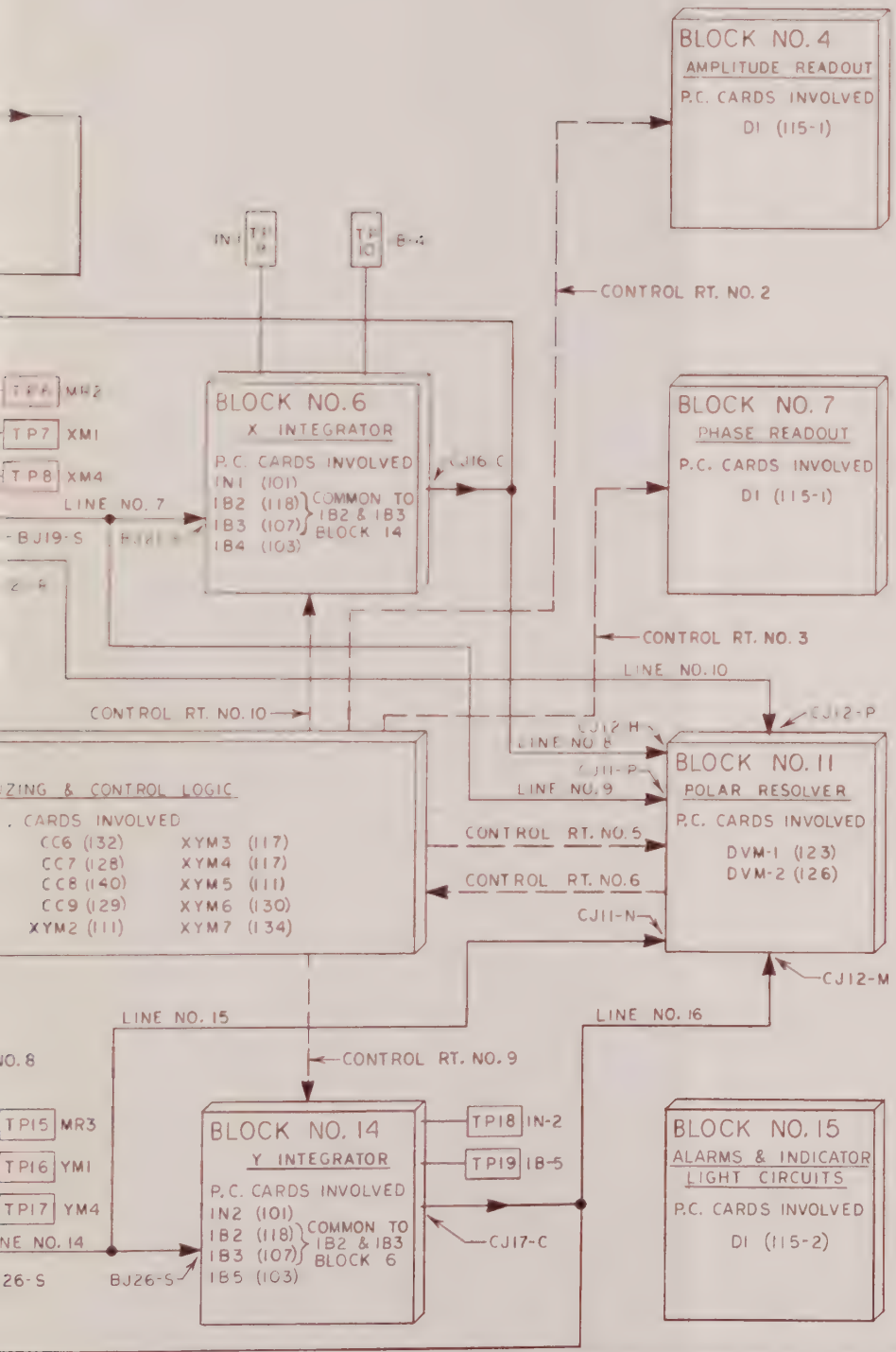
WIRING DIAGRAM SUB PANEL

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC

DRAWING NUMBER: 801-5-01-600
REV.: 7


5V
.95V
5V
15V
D.C. CONTROL
3600 PPS
CARRIER INPUT
M01 TP 1
M03 TP 2
FG1 TP 3
FG4 TP 4
FG5
OA2 TP 5
BJ5-S
BLOCK NO. 1
MASTER OSCILLATOR
P.C. CARDS INVOLVED
M01 (135)
M02 (120)
M03 (102)
M04 (136)
M05 (137)
FRONT PANEL CONTROL
LINE NO. 1
CJ4-R
BJ-6-T
BJ-7-T
BJ-8-T
BJ-9-T
BLOCK NO. 2
FUNCTION GENERATOR
P.C. CARDS INVOLVED
FG1 (142)
FG2 (106)
FG3 (105)
FG4 (121)
FG5 (127)
FG6 (117)
FG7 (117)
FG8 (114)
FG9 (119)
OA1 (108)
OA2 (100)
CJ2-H
OUTPUT JACK
LINE NO. 2
BLOCK NO. 3
EXTERNAL SYSTEM UNDER TEST
LINE NO. 3
LINE NO. 5
200NS - 10 μSEC.
.0036 KHZ - 3.6 MHZ
5V
CONTROL ROUTE NO. 1
LINE NO. 4
BLOCK NO. 5
X MULTIPLIER (SINE)
P.C. CARDS INVOLVED
MR2 (116)
XM1 (121)
XM2 (105)
XM3 (106)
XM4 (145)
XYM1 (109)
CJ21-F
LINE NO. 6
.6V
2.4V
.6V
CONTROL ROUTE NO. 7
IA1 TP 11
IA2 TP 12
IA3 TP 13
IA4 TP 14
LINE NO. 3
CJ18-P
CJ18-S
BLOCK NO. 8
INPUT AMPLIFIER
P.C. CARDS INVOLVED
IA1 (110)
IA2 (141)
IA3 (110)
IA4 (148)
INPUT JACK
LINE NO. 11
CJ25-M
CJ18-R
BLOCK NO. 9
MULTIPLIER ROUTING
P.C. CARDS INVOLVED
MR1 (125)
CONTROL RT. NO. 4
BLOCK NO. 10
SYNCH
CONTROL
CJ18-N
CJ18-M
BLOCK NO. 12
POWER SUPPLY
P.C. CARDS INVOLVED
+5V REG. (147)
±20V REG. (122)
OUTPUT VOLTAGES
+5V REGULATED
+20V REGULATED
-20V REGULATED
+180V UNREGULATED
BLOCK NO. 13
Y MULTIPLIER (COSINE)
P.C. CARDS INVOLVED
MR3 (116)
YM1 (121)
YM2 (105)
YM3 (106)
YM4 (145)
LINE NO. 12
CJ22-P
LINE NO. 13

NO.	REVISION	BY	CHK	APP	DATE



P.C. CARD DESIGNATIONS NUMBER IN PARENTHESIS INDICATES SCHEMATIC DRAWING NUMBER.

EXAMPLE:
MO1 (135) = MASTER OSCILLATOR-
DWG. NO. 881-5-01-135.

FIRST RELEASE-DRN 003, ?

		THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC. AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION, SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST.	DATE APRIL 11, 1968	UNSPECIFIED TOLERANCE	OVERALL BLOCK DIAGRAM DA1410
			DR. E. BACHMAYER	THREE DEC. PLCS. ±.005	
			CHK.	TWO DEC. PLCS. ±.010	
			APP.	FRACTIONS ±1/64	
			APP.	ANGLES ±0°-30'	
			MATL.	FINISH	

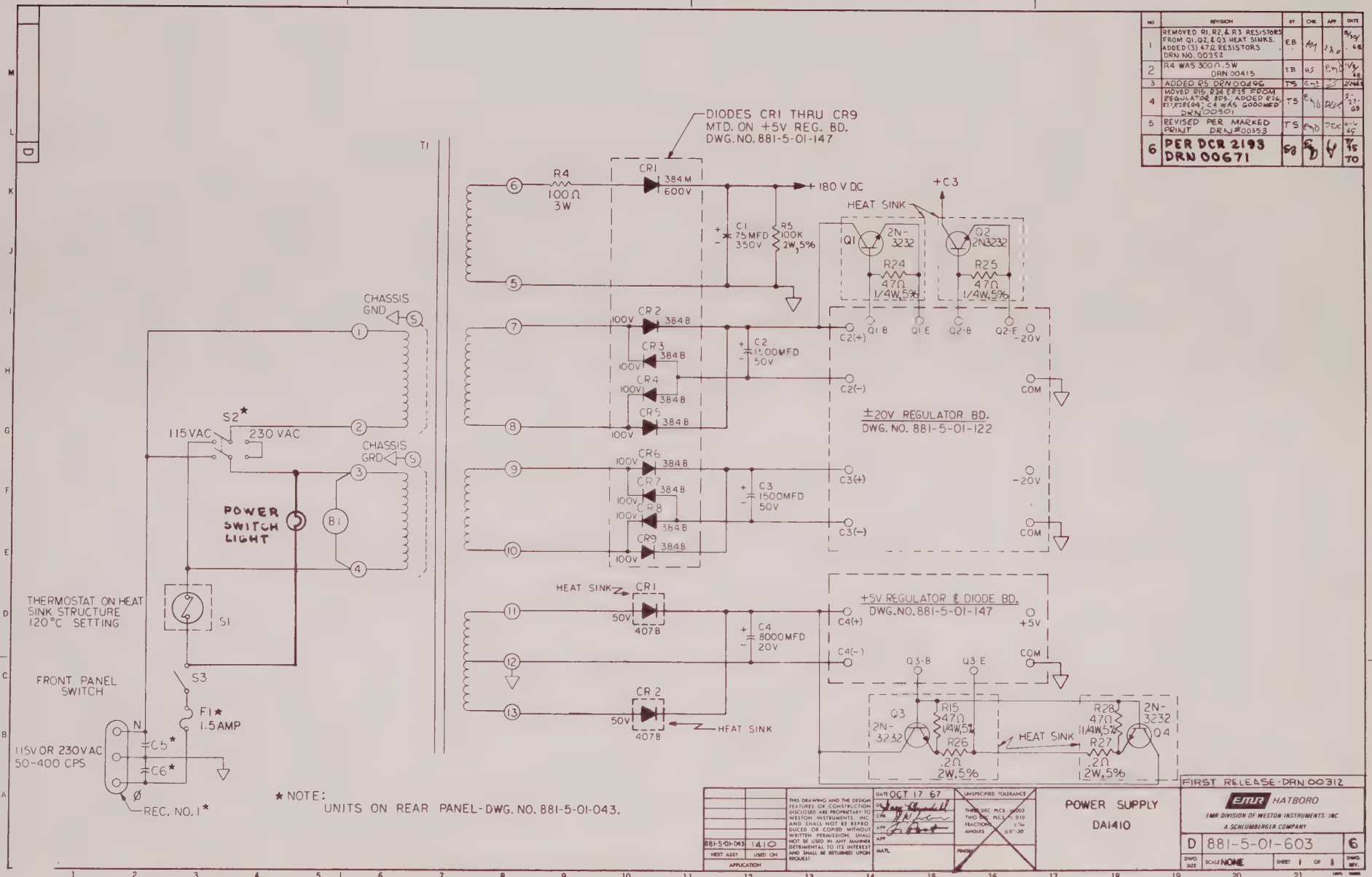
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

NEXT ASSY.	USED ON
	1410
APPLICATION	

DWG SIZE	SCALE	SHEET	OF	DWG. REV.
D	881-5-01-602			0

12 13 14 15 16 17 18 19 20 21

1DF4 80268



NO	REVISION	BY	CHK	APP	DATE
1	REMOVED R1, R2, & R3 RESISTORS FROM Q1, Q2, & Q3 HEAT SINKS. ADDED (3) 47Ω RESISTORS DRN NO. 00352	EB			8/29/68
2	R4 WAS 300Ω, 5W DRN 00415	EB			10/9/68
3	ADDED R5 DRN 00496	TS			2/14/69
4	MOVED R15, R24 & R25 FROM REGULATOR BD'S. ADDED R26, R27, R28 & Q4; C4 WAS 6000 MFD DRN 00501	TS			2-27-69
5	REVISED PER MARKED PRINT DRN #00553	TS			6-6-69
6	PER DCR 2193 DRN 00671	SB			7/15/70

★NOTE:
UNITS ON REAR PANEL - DWG. NO. 881-5-01-043.

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DATE OCT 17 67
CHK
APP
APP
MATL

UNSPECIFIED TOLERANCE
THREE DEC PLCS ±.005
TWO DEC PLCS ±.010
FRACTIONS ±1/64
ANGLES ±0°-30'
FINISH

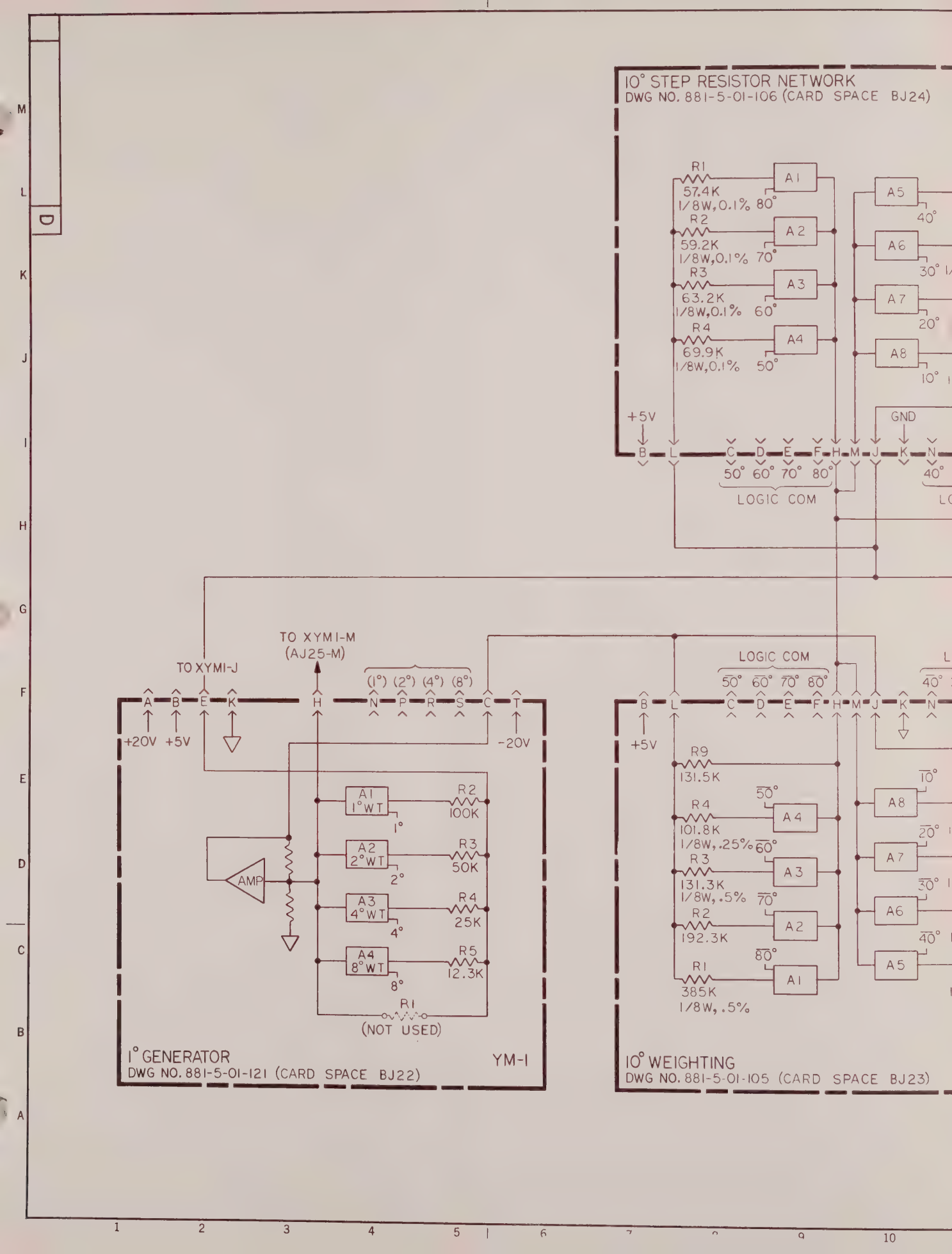
881-5-01-043 1410
NEXT ASSY USED ON
APPLICATION

POWER SUPPLY
DA1410

FIRST RELEASE - DRN 00312

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

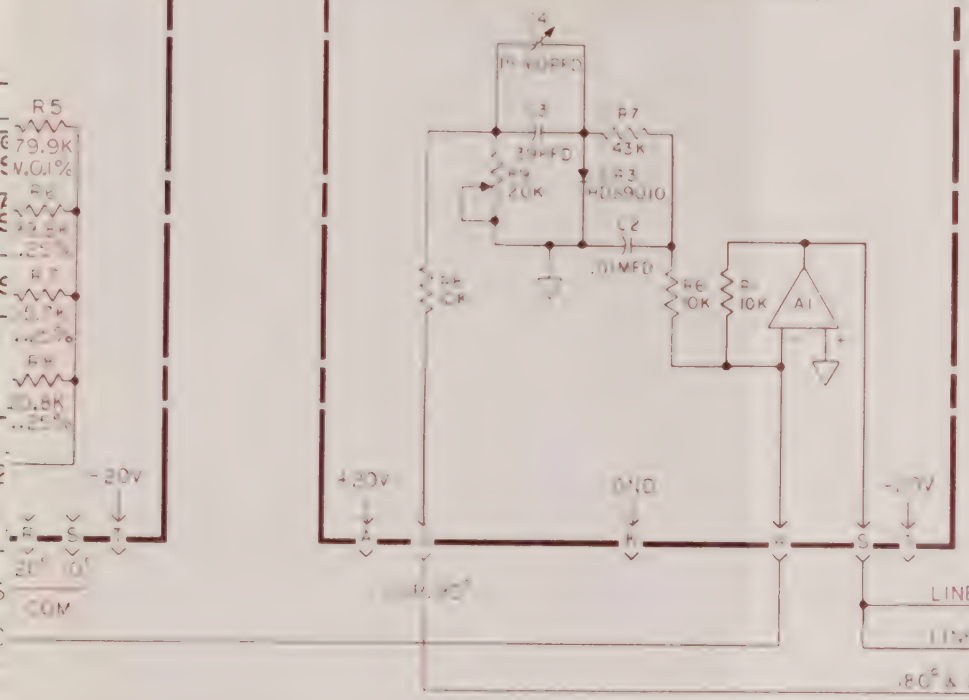
D 881-5-01-603 6
DWG SIZE SCALE NONE SHEET 1 OF 1 DWG. REV.

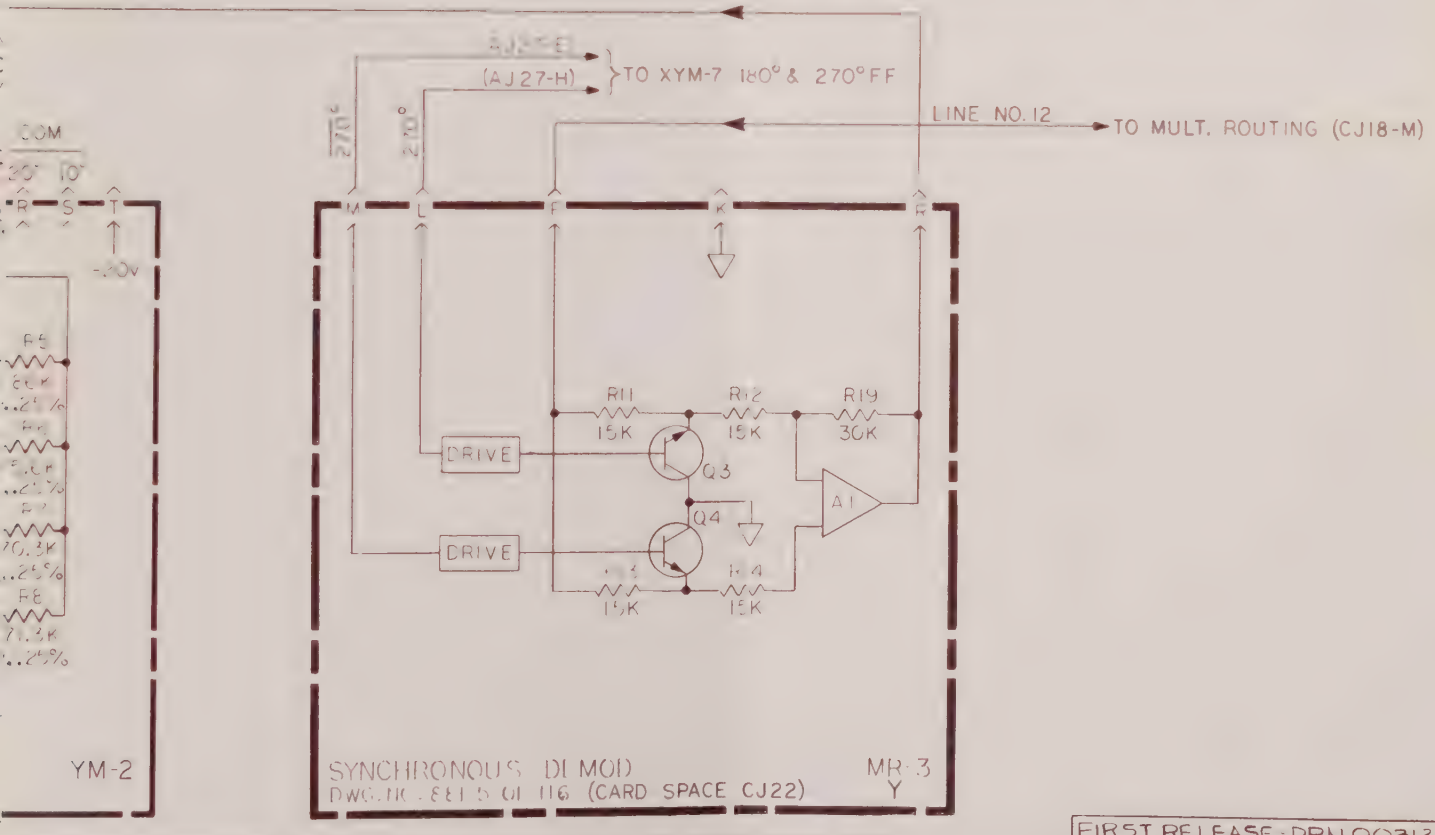

10° STEP RESISTOR NETWORK
DWG NO. 881-5-01-106 (CARD SPACE BJ24)
R1
57.4K
1/8W,0.1% 80°
R2
59.2K
1/8W,0.1% 70°
R3
63.2K
1/8W,0.1% 60°
R4
69.9K
1/8W,0.1% 50°
A1
A2
A3
A4
A5
40°
A6
30°
A7
20°
A8
10°
+5V
GND
B L C D E F H M J K N
50° 60° 70° 80°
LOGIC COM
40°
TO XYM1-M
(AJ25-M)
TO XYM1-J
(1°) (2°) (4°) (8°)
A B E K H N P R S C T
+20V +5V -20V
A1
1°WT
1°
R2
100K
A2
2°WT
2°
R3
50K
A3
4°WT
4°
R4
25K
A4
8°WT
8°
R5
12.3K
AMP
R1
(NOT USED)
1° GENERATOR
DWG NO. 881-5-01-121 (CARD SPACE BJ22)
YM-1
LOGIC COM
50° 60° 70° 80°
B L C D E F H M J K N
+5V
R9
131.5K
R4
101.8K
1/8W,.25%
R3
131.3K
1/8W,.5%
R2
192.3K
R1
385K
1/8W,.5%
10° WEIGHTING
DWG NO. 881-5-01-105 (CARD SPACE BJ23)

NO	REVISION	BY	CHK	APP.	DATE

YM-3

SUMMATION AMPLIFIER M-4
DWG NO. 881-5-01-145 (CARD SPACE BJ26)





YM-2

SYNCHRONOUS DEMOD
DWG. NO. 881-5-01-116 (CARD SPACE CJ22)
MR-3
Y

FIRST RELEASE - DRN 00312

		DATE	30 AUG 67	UNSPECIFIED TOLERANCE	
		DR.	FK	THREE DEC. PLCS. ±.005	BLOCK & INTERCONNECTION DIAGRAM Y-MULTIPLIER ANALOG CIRCUITRY DAI410
		CHK		TWO DEC. PLCS. .010	
		APP.		FRACTIONS ±1/64	
		APP		ANGLES ±0°-30'	
		MATL.		FINISH	
NEXT ASSY	USED ON				
APPLICATION	410				

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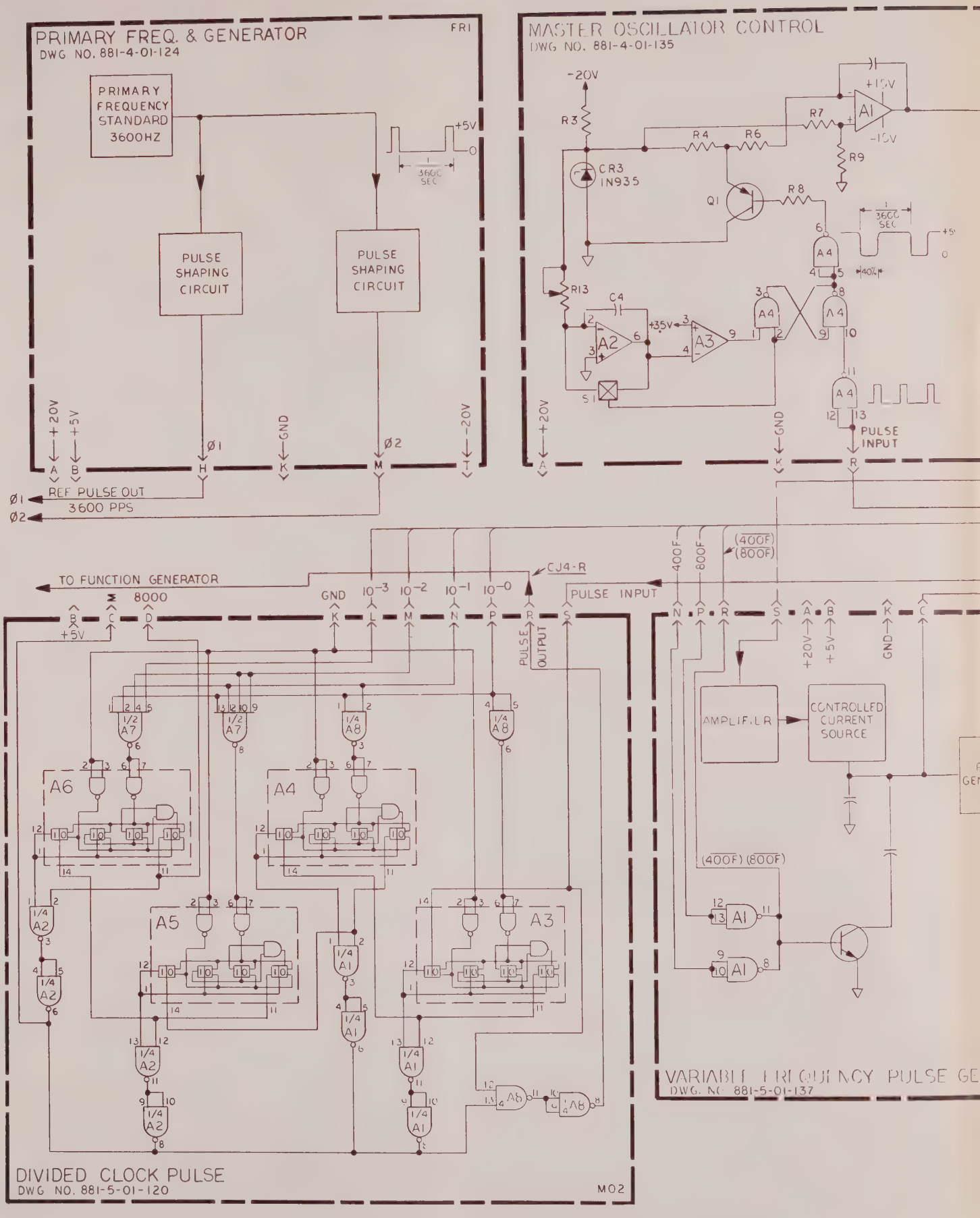
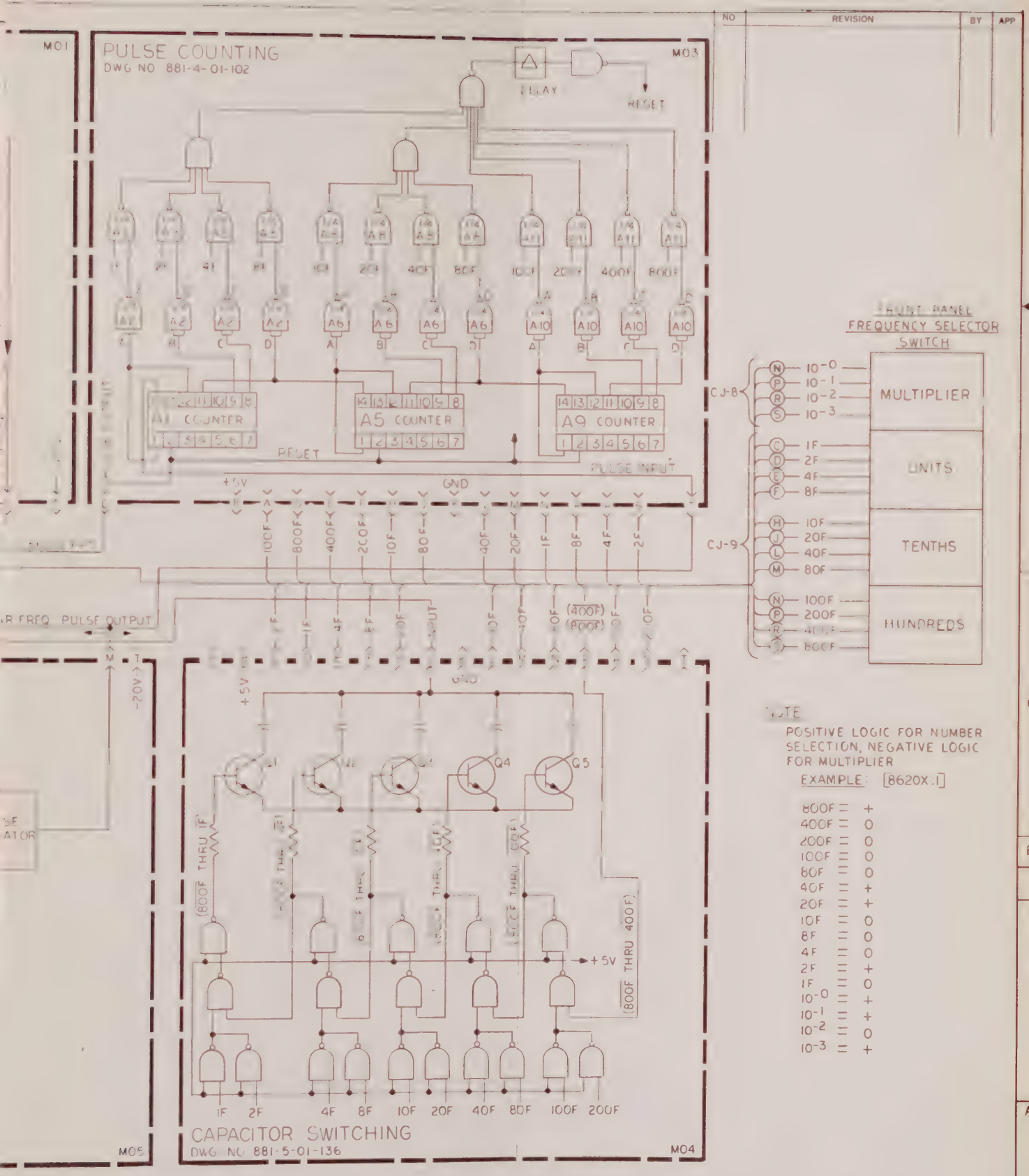
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

DWG SIZE		SCALE	SHEET	OF	DWG. REV.
D	881-5-01-604	~	1	1	0

1DF4 80235

12 13 14 15 16 17 18 19 20 21


PRIMARY FREQ. & GENERATOR
DWG NO. 881-4-01-124
FRI
PRIMARY FREQUENCY STANDARD 3600HZ
PULSE SHAPING CIRCUIT
PULSE SHAPING CIRCUIT
+5V
0
1/3600 SEC
+20V
+5V
GND
-20V
Ø1
Ø2
REF PULSE OUT
3600 PPS
MASTER OSCILLATOR CONTROL
DWG NO. 881-4-01-135
-20V
+15V
-15V
R3
R4
R6
R7
R8
R9
R13
C4
CR3 IN935
Q1
A1
A2
A3
A4
S1
+35V
1/3600 SEC
40%
PULSE INPUT
TO FUNCTION GENERATOR
8000
GND
10-3
10-2
10-1
10-0
CJ4-R
PULSE OUTPUT
PULSE INPUT
400F
800F
(400F) (800F)
AMPLIFIER
CONTROLLED CURRENT SOURCE
A6
A4
A5
A3
A7
A8
A2
A1
DIVIDED CLOCK PULSE
DWG NO. 881-5-01-120
M02
VARIABLE FREQUENCY PULSE GE
DWG. NO. 881-5-01-137



NO	REVISION	BY	APP

NOTE

POSITIVE LOGIC FOR NUMBER SELECTION, NEGATIVE LOGIC FOR MULTIPLIER

EXAMPLE: [8620X.1]

800F	=	+
400F	=	0
200F	=	0
100F	=	0
80F	=	0
40F	=	+
20F	=	+
10F	=	0
8F	=	0
4F	=	0
2F	=	+
1F	=	0
10^{-0}	=	+
10^{-1}	=	+
10^{-2}	=	0
10^{-3}	=	+

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NEXT ASSY	1410
USED ON	

PROJECT NO:	
DATE:	
DRAWN:	
CHECKED:	
APPROVED:	
SCALE:	

UNSPECIFIED TOLERANCE
TWO DEC. PLACES ± .010
THREE DEC. PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0° 30'

MATERIAL:
PROTECTIVE FINISH:
QUANT. PER. ASSY:

FIRST RELEASE - DRN00312

BLOCK & INTERCONNECTION DIAGRAM MASTER OSCILLATOR-DA1410

EMR HATBORO
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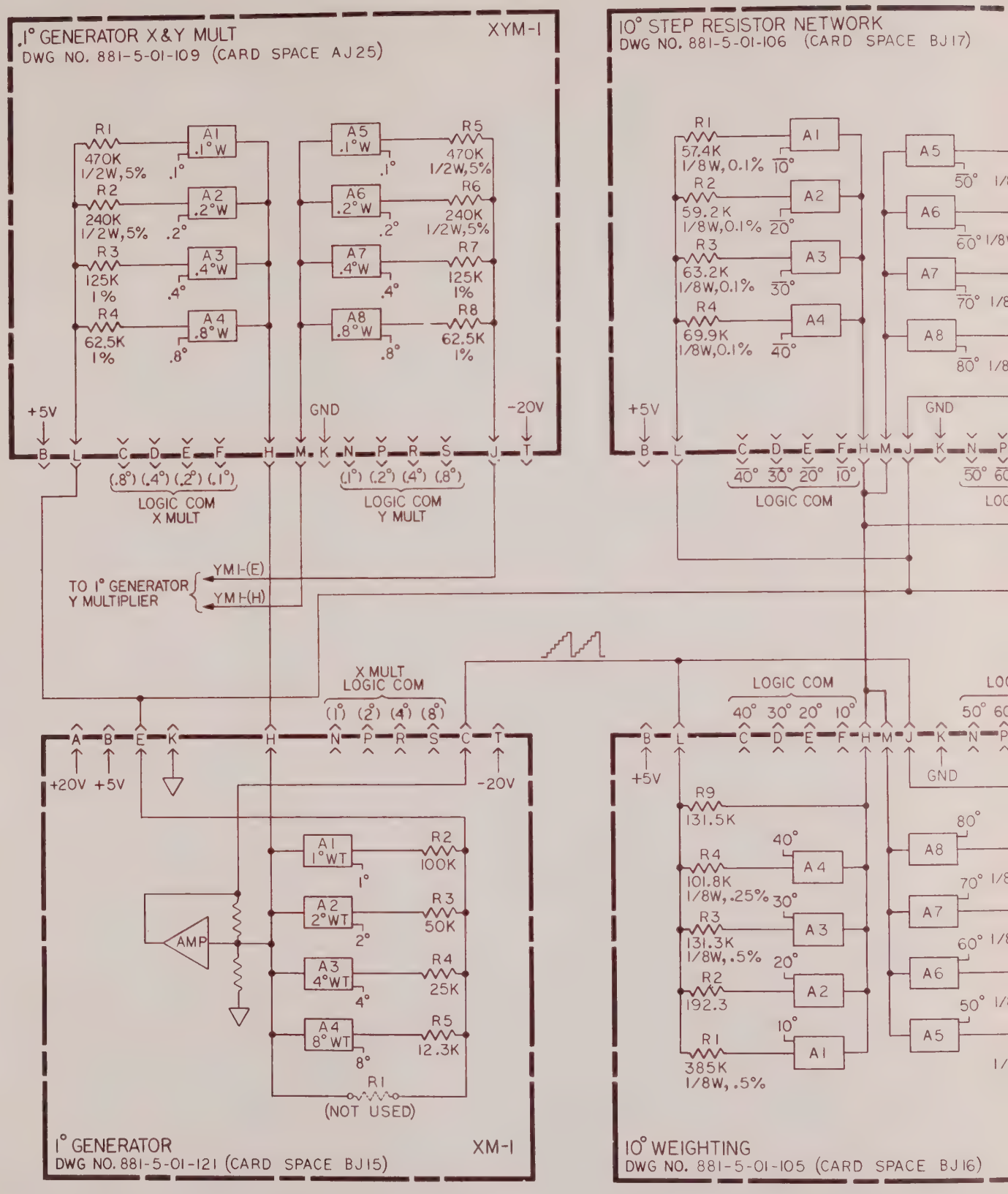
DRAWING NUMBER	REV.
881-5-01-607	0

3 2 1

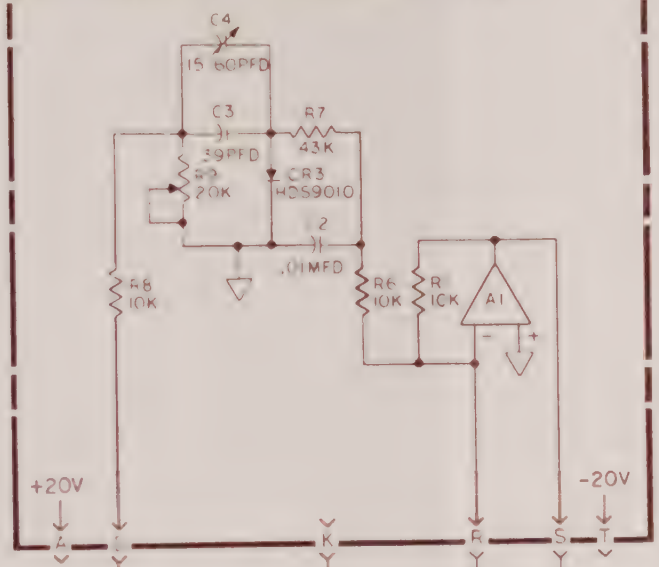

.1° GENERATOR X&Y MULT
DWG NO. 881-5-01-109 (CARD SPACE AJ25)
XYM-1
R1 470K 1/2W,5%
R2 240K 1/2W,5%
R3 125K 1%
R4 62.5K 1%
A1 .1°W
A2 .2°W
A3 .4°W
A4 .8°W
A5 .1°W
A6 .2°W
A7 .4°W
A8 .8°W
R5 470K 1/2W,5%
R6 240K 1/2W,5%
R7 125K 1%
R8 62.5K 1%
+5V
GND
-20V
B L C D E F H M K N P R S J T
(.8°) (.4°) (.2°) (.1°)
LOGIC COM X MULT
(.1°) (.2°) (.4°) (.8°)
LOGIC COM Y MULT
TO 1° GENERATOR Y MULTIPLIER
YM1-(E)
YM1-(H)
10° STEP RESISTOR NETWORK
DWG NO. 881-5-01-106 (CARD SPACE BJ17)
R1 57.4K 1/8W,0.1%
R2 59.2K 1/8W,0.1%
R3 63.2K 1/8W,0.1%
R4 69.9K 1/8W,0.1%
A1 10°
A2 20°
A3 30°
A4 40°
A5 50°
A6 60°
A7 70°
A8 80°
+5V
GND
B L C D E F H M J K N P
40° 30° 20° 10°
LOGIC COM
X MULT LOGIC COM
(1°) (2°) (4°) (8°)
A B E K H N P R S C T
+20V +5V -20V
AMP
A1 1°WT R2 100K
A2 2°WT R3 50K
A3 4°WT R4 25K
A4 8°WT R5 12.3K
R1 (NOT USED)
1° GENERATOR
DWG NO. 881-5-01-121 (CARD SPACE BJ15)
XM-1
LOGIC COM
40° 30° 20° 10°
B L C D E F H M J K N P
+5V
GND
R9 131.5K
R4 101.8K 1/8W,.25%
R3 131.3K 1/8W,.5%
R2 192.3
R1 385K 1/8W,.5%
A4 40°
A3 30°
A2 20°
A1 10°
A8 80°
A7 70°
A6 60°
A5 50°
10° WEIGHTING
DWG NO. 881-5-01-105 (CARD SPACE BJ16)

NO	REVISION	BY	CHK.	APP.	DATE

XM-3

SUMMATION AMPLIFIER
DWG NO. 881-5-01-145 (CARD SPACE BJ19)

XM-4



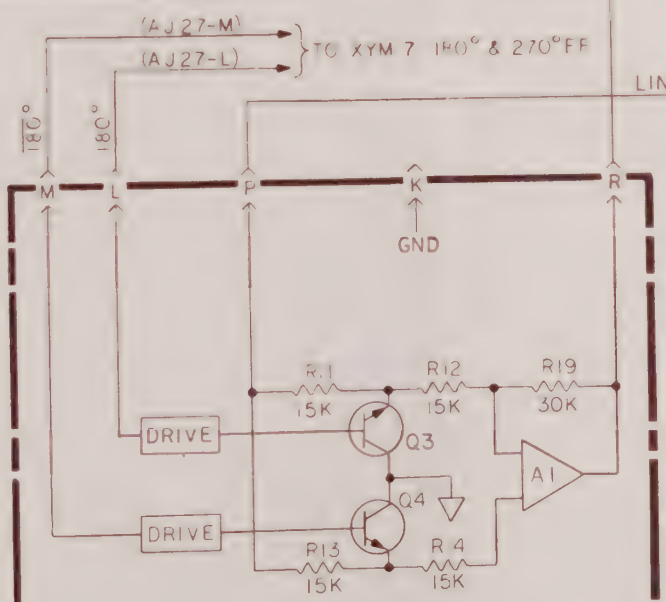
LINE NO. 9 → TO BLOCK NO. 11 (CJ11-P)

LINE NO. 7 → TO X INTEGRATOR (BJ21-S)

180° & 270° FF → TO XYM-7 (AJ27-J)

(AJ27-M)
(AJ27-L)
} TO XYM 7 180° & 270° FF

LINE NO. 6 → TO MULT. ROUTING (CJ18-S)



SYNCHRONOUS DEMOD
DWG. NO. 881 5 01 116 (CARD SPACE CJ21)

MR-2
X

XM-2

FIRST RELEASE-DRN00312

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EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

BLOCK & INTERCONNECTION DIAGRAM X-MULTIPLIER ANALOG CIRCUITRY DA1410

D | 881-5-01-605 | 0

DWG. SIZE | SCALE NONE | SHEET 1 OF 1 | DWG. REV.

1 OF 4 80235

NEXT ASSY. 1410 | USED ON

APPLICATION

DATE 1 SEPT 67
DR. FK
CHK H N Sobin
APP. F Post
APP
MATL.
FINISH

UNSPECIFIED TOLERANCE
THREE DEC. PLCS. ±.005
TWO DEC. PLCS. ±.010
FRACTIONS ±1/64
ANGLES ±0°-30'

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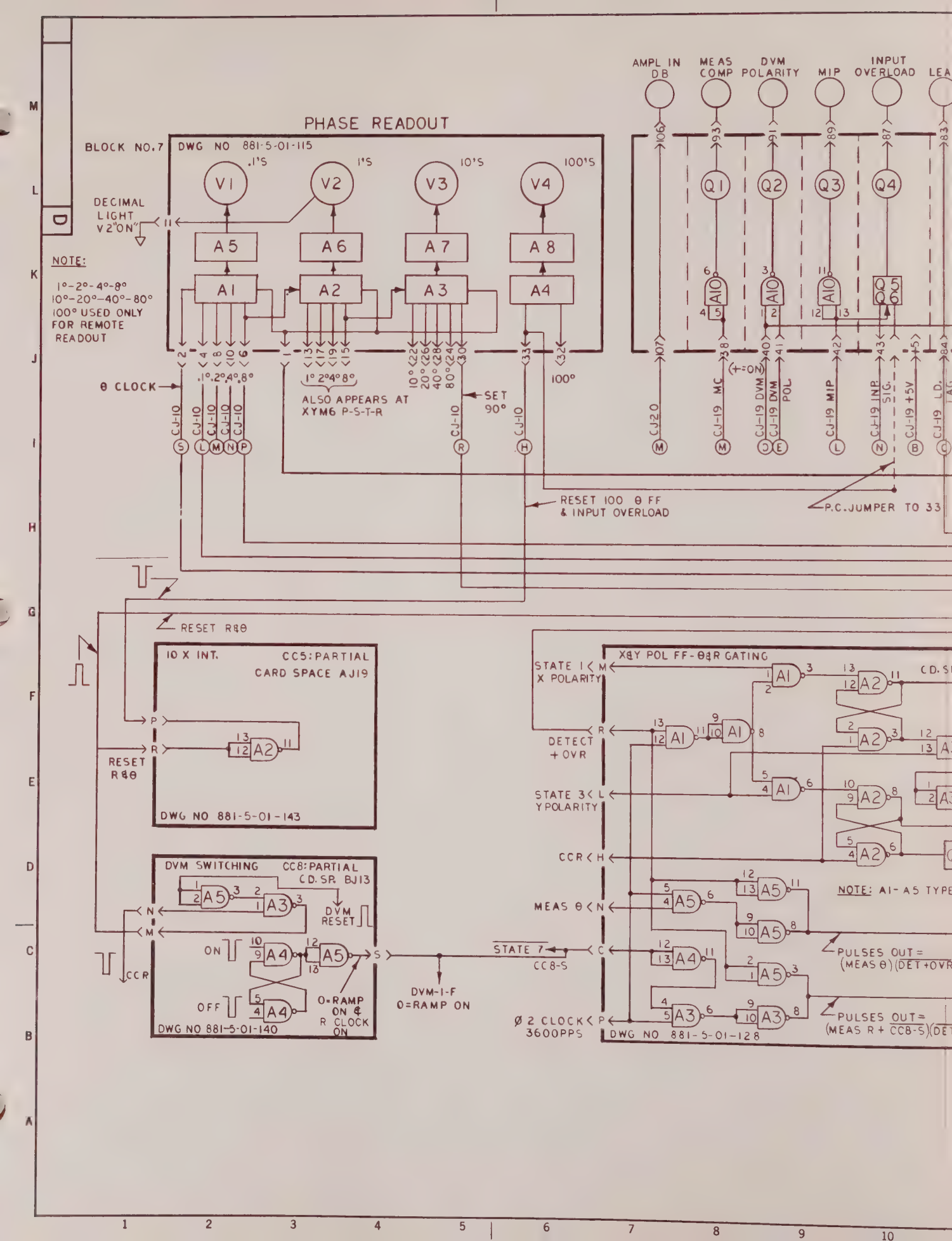
12 13 14 15 16 17 18 19 20 21


PHASE READOUT
BLOCK NO.7
DWG NO 881-5-01-115
.1'S
1'S
10'S
100'S
V1
V2
V3
V4
DECIMAL LIGHT V2 "ON"
A5
A6
A7
A8
A1
A2
A3
A4
NOTE:
1°-2°-4°-8°
10°-20°-40°-80°
100° USED ONLY FOR REMOTE READOUT
θ CLOCK
.1°.2°.4°.8°
1° 2°4°8°
ALSO APPEARS AT XYM6 P-S-T-R
10° 20° 40° 80°
SET 90°
100°
CJ-10
CJ-20
CJ-19 MC
CJ-19 DVM POL
CJ-19 MIP
CJ-19 INP SIG.
CJ-19 +5V
CJ-19 LD.
AMPL IN DB
MEAS COMP
DVM POLARITY
MIP
INPUT OVERLOAD
LEA
Q1
Q2
Q3
Q4
Q5 Q6
A10
(+=ON)
RESET 100 θ FF & INPUT OVERLOAD
P.C. JUMPER TO 33
RESET RθΘ
10 X INT.
CC5: PARTIAL CARD SPACE AJ19
RESET RθΘ
DWG NO 881-5-01-143
DVM SWITCHING
CC8: PARTIAL CD. SR. BJ13
DVM RESET
ON
OFF
CCR
0=RAMP ON & R CLOCK ON
DWG NO 881-5-01-140
DVM-1-F
0=RAMP ON
STATE 7
CC8-S
XθY POL FF-θθR GATING
STATE 1
X POLARITY
DETECT +OVR
STATE 3
Y POLARITY
CCR
MEAS θ
Ø 2 CLOCK 3600PPS
NOTE: A1-A5 TYPE
PULSES OUT = (MEAS θ)(DET+OVR
PULSES OUT = (MEAS R + CC8-S)(DE
DWG NO 881-5-01-128

NO	REVISION	BY	CHK.	APP	DATE
	REVISED PER MARKED PRINT DRN	TS			

POWER OVERLOAD

95 79

R11 R10

BLOCK NO 15 DWG NO 881-5-01-115

LIGHTS ON

TO +5V REG. BD.

AMPLITUDE READOUT

BLOCK NO.4 DWG NO 881-5-01-115

1'S 10'S 100'S 1000'S

V1A V2A V3A V4A

A5A A6A A7A A8A

A1A A2A A3A A4A

1 2 4 8

R CLOCK

RESET P&P COUNTERS

RANGE 1
RANGE 2
RANGE 3
RANGE 4

DECIMAL DECK

INPUT RANGE SWITCH

NOTE:
1-2-4-8
10-20-40-80
100-200-400-800
1000-2000-4000-8000
USED ALSO FOR REMOTE READOUT

DETECT SWITCHING LOGIC

CC9
CARD SPACE BJ14

80° COR
8° COR
1° COR
.8° COR
.1° COR
MEAS θ
+5V
1000
600
100
MEAS R
DVM
DETECT

A1 830
A2 833
A3 846

(DETECT)ø(OVER-RANGE)

WIRING TABLE

80° COR	TO XYM4-R
8° COR	TO XYM6-R
1° COR	TO XYM6-P
MEAS θ	TO CC6-M
DETECT	TO DVM-2-J
MEAS R	TO CC6-R

R8θ
DVM CAL
FRONT PANEL MODE SWITCH

0=ON

DWG NO 881-5-01-129

0=ON → TO CC8-L

FIRST RELEASE - DRN 00312

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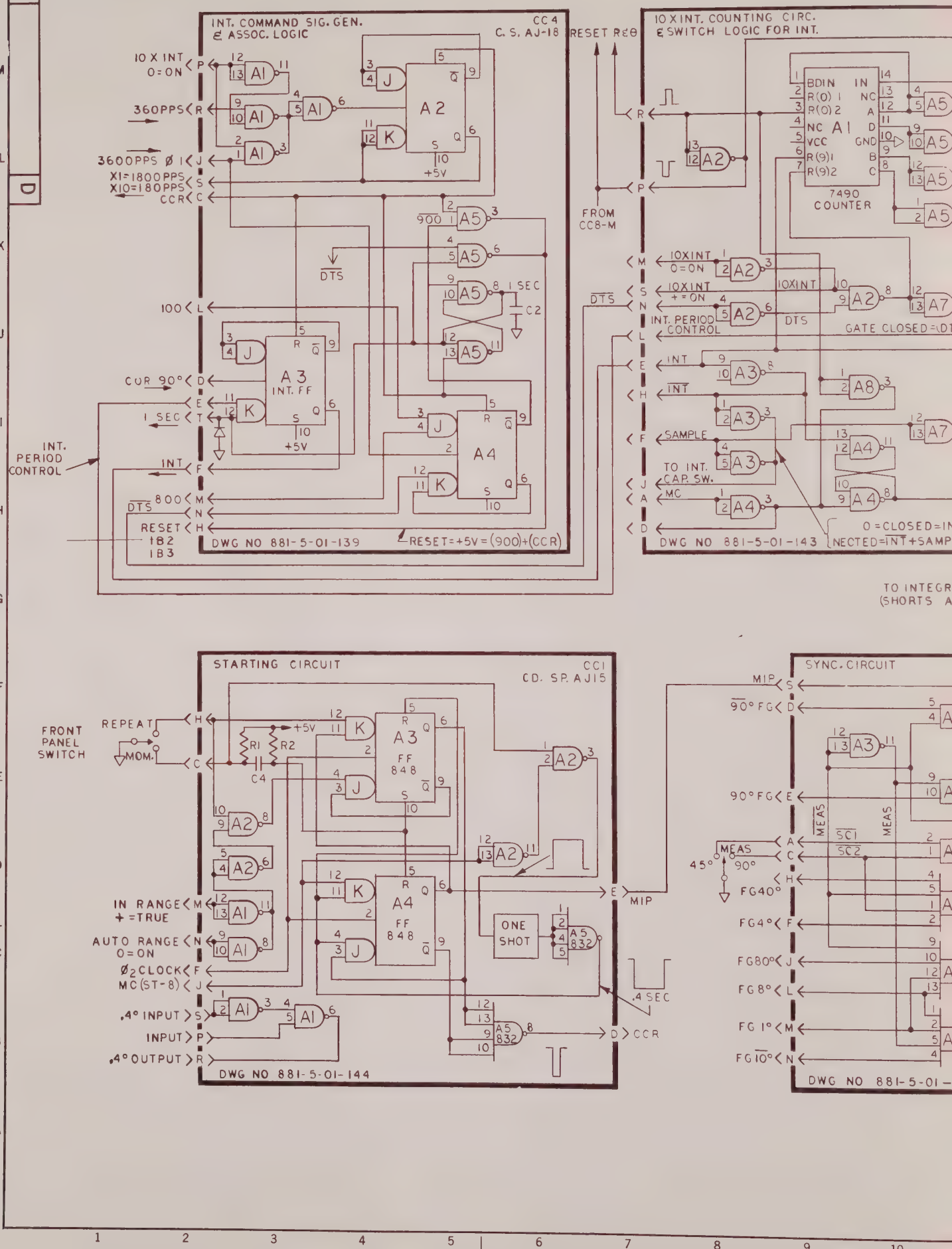
			DR T. SMITH	THREE DEC. PLCS. ±.005	
			CHK	TWO DEC. PLCS. ±.010	
			APP.	FRACTIONS ±1/64	
			APP.	ANGLES ±0°-30'	
	1410		MATL	FINISH	
NEXT ASSY.	USED ON				
APPLICATION					

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

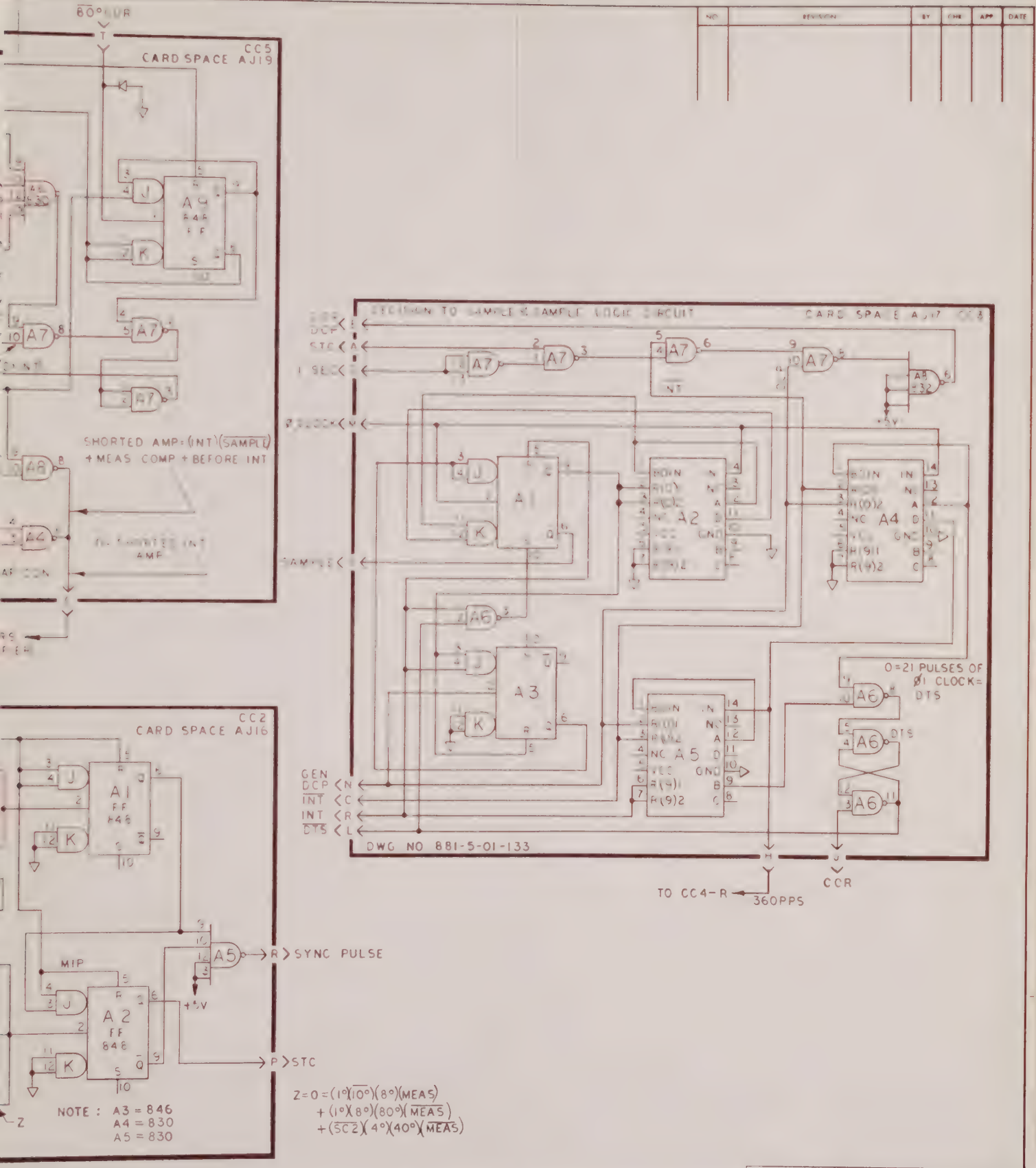
D	881-5-01-609	1
DWG SIZE	SCALE	SHEET 1 OF 1	DWG. REV.

11 12 13 14 15 16 17 18 19 20 21

1 OF 4 80268


INT. COMMAND SIG. GEN. & ASSOC. LOGIC
CC4
C. S. AJ-18
10 X INT 0=ON
360PPS
3600PPS Ø 1
X1=1800PPS
X10=180PPS
CCR
DTS
100
CUR 90°
1 SEC
INT.
PERIOD
CONTROL
INT
800
RESET
1B2
1B3
A1
A2
A3
INT. FF
A4
A5
J
K
R
S
Q
+5V
C2
1 SEC
DWG NO 881-5-01-139
RESET=+5V=(900)+(CCR)
RESET REØ
FROM CC8-M
10 X INT. COUNTING CIRC. & SWITCH LOGIC FOR INT.
BDIN
R(0) 1
R(0) 2
NC A1
VCC
R(9)1
R(9)2
IN
NC
A
D
GND
B
C
7490 COUNTER
10XINT 0=ON
10XINT += ON
INT. PERIOD CONTROL
10XINT
DTS
GATE CLOSED=\DT
INT
SAMPLE
TO INT. CAP. SW.
MC
A7
A8
0=CLOSED=IN
NECTED=INT+SAMP
DWG NO 881-5-01-143
TO INTEGR
(SHORTS A
STARTING CIRCUIT
CC1
CD. SP. AJ15
FRONT PANEL SWITCH
REPEAT
MOM.
R1
R2
C4
+5V
IN RANGE + =TRUE
AUTO RANGE 0=ON
Ø2 CLOCK
MC (ST-8)
.4° INPUT
INPUT
.4° OUTPUT
FF 848
ONE SHOT
A5 832
MIP
.4 SEC
CCR
DWG NO 881-5-01-144
SYNC. CIRCUIT
MIP
90° FG
90° FG
MEAS
SC1
SC2
45°
90°
FG40°
FG4°
FG80°
FG8°
FG 1°
FG 10°
DWG NO 881-5-01-

NO	REVISION	BY	CHK	APP	DATE



FIRST RELEASE-DRN00312

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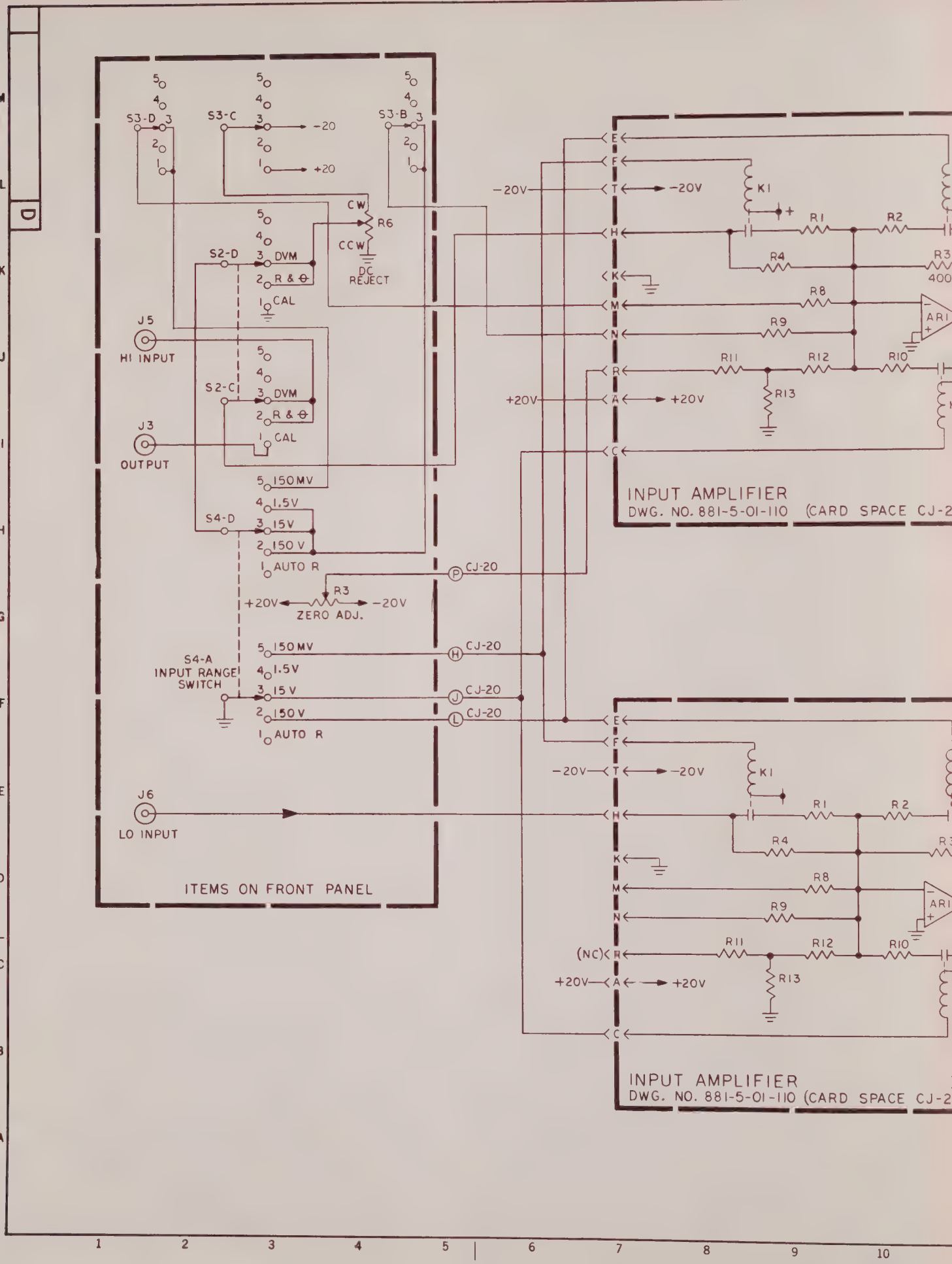
			DR. T. SMITH	THREE DEC. PLCS. ±.005	CC1-CC2-CC3
			CHK.	TWO DEC. PLCS. ±.010	CC4-CC5
			APP.	FRACTIONS ±1/64	
			APP.	ANGLES ±0°-30'	
	DA1410		MATL.	FINISH	
NEXT ASSY.	USED ON				
APPLICATION					

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

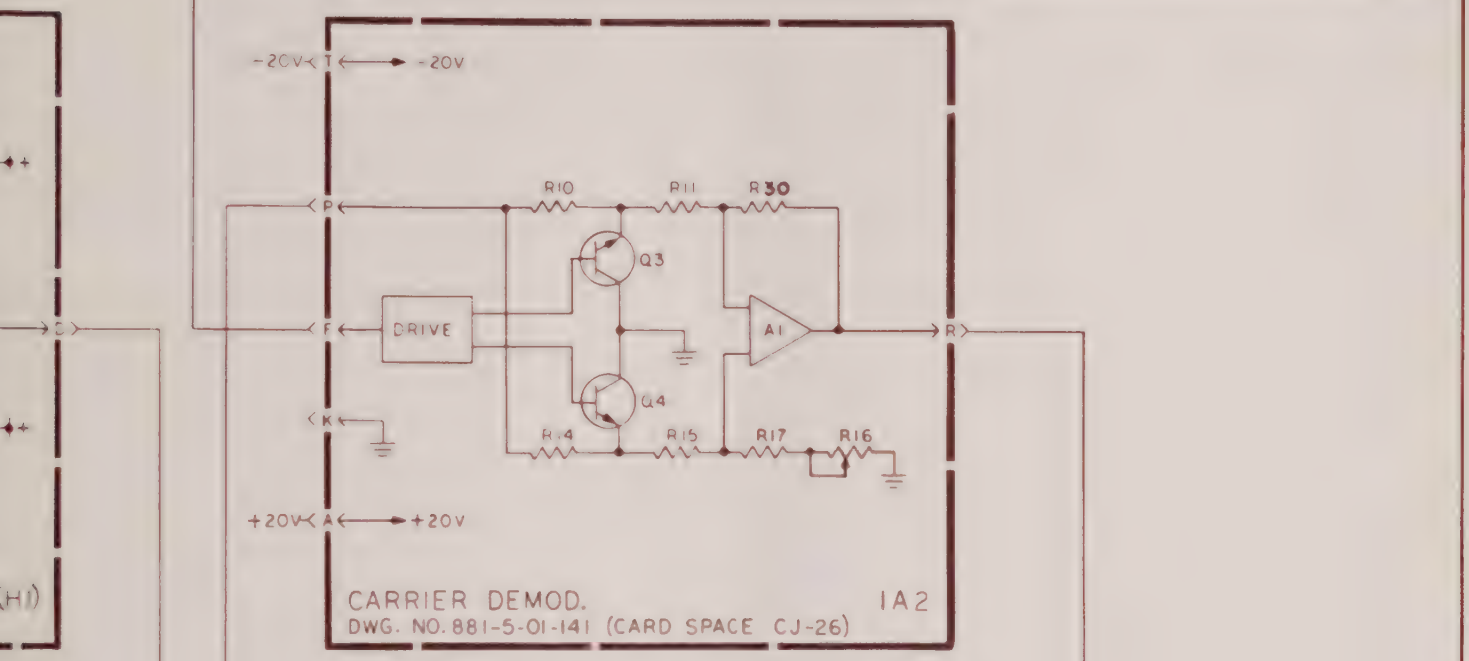
D	881-5-01-610	0
DWG. SIZE	SCALE	SHEET 1 OF 1	DWG. REV.

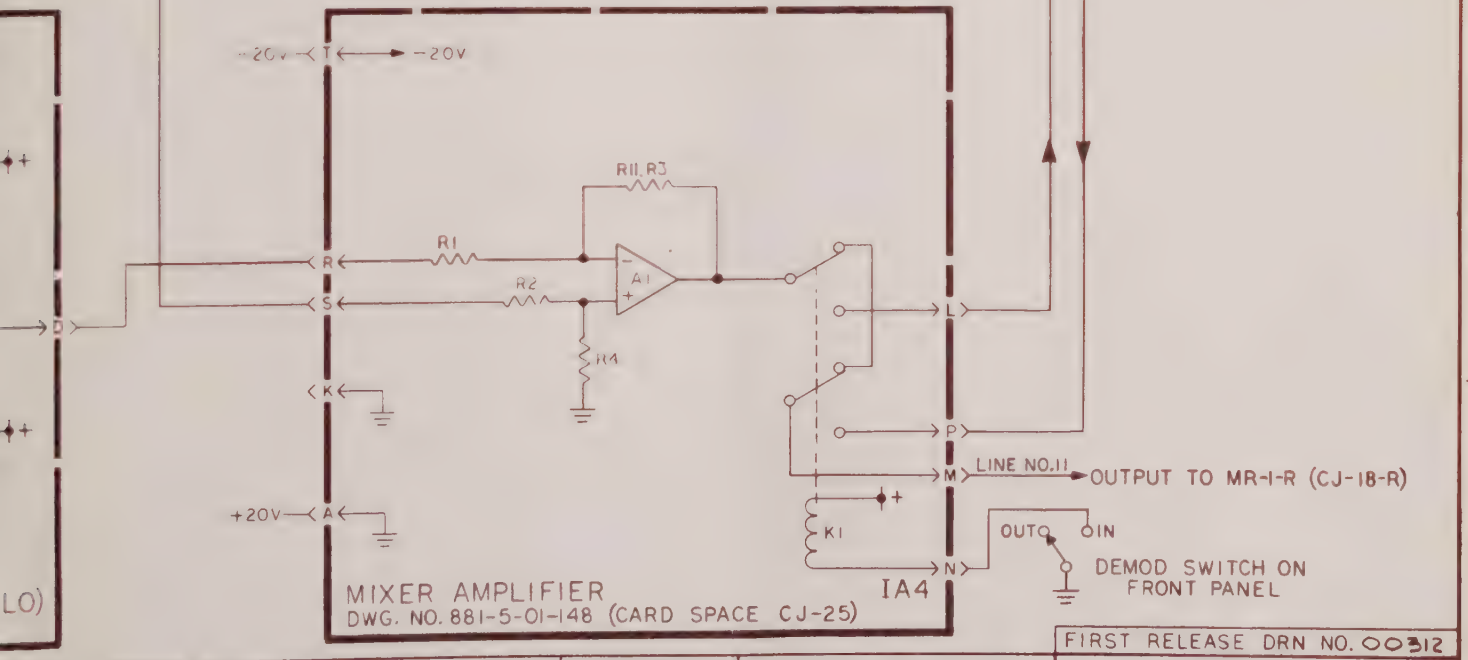
12 13 14 15 16 17 18 19 20 21


S3-D
S3-C
S3-B
-20
+20
CW
R6
CCW
DC REJECT
S2-D
DVM
R & Θ
CAL
J5
HI INPUT
S2-C
J3
OUTPUT
150MV
1.5V
15V
150V
AUTO R
S4-D
R3
+20V
ZERO ADJ.
-20V
S4-A
INPUT RANGE
SWITCH
CJ-20
J6
LO INPUT
ITEMS ON FRONT PANEL
-20V
+20V
K1
R1
R2
R3
400
R4
R8
R9
R10
R11
R12
R13
AR1
INPUT AMPLIFIER
DWG. NO. 881-5-01-110 (CARD SPACE CJ-2
(NC)

NO.	REVISION	BY	CHK.	APP.	DATE
1	REVISED S2 WIRING DRN 00441	CPA			
2	REVISED PER MARKED PRINT DRN #00532				
3	DRN 00641	TS			

TO FG-1-C (BJ1-C)





FIRST RELEASE DRN NO. 00312

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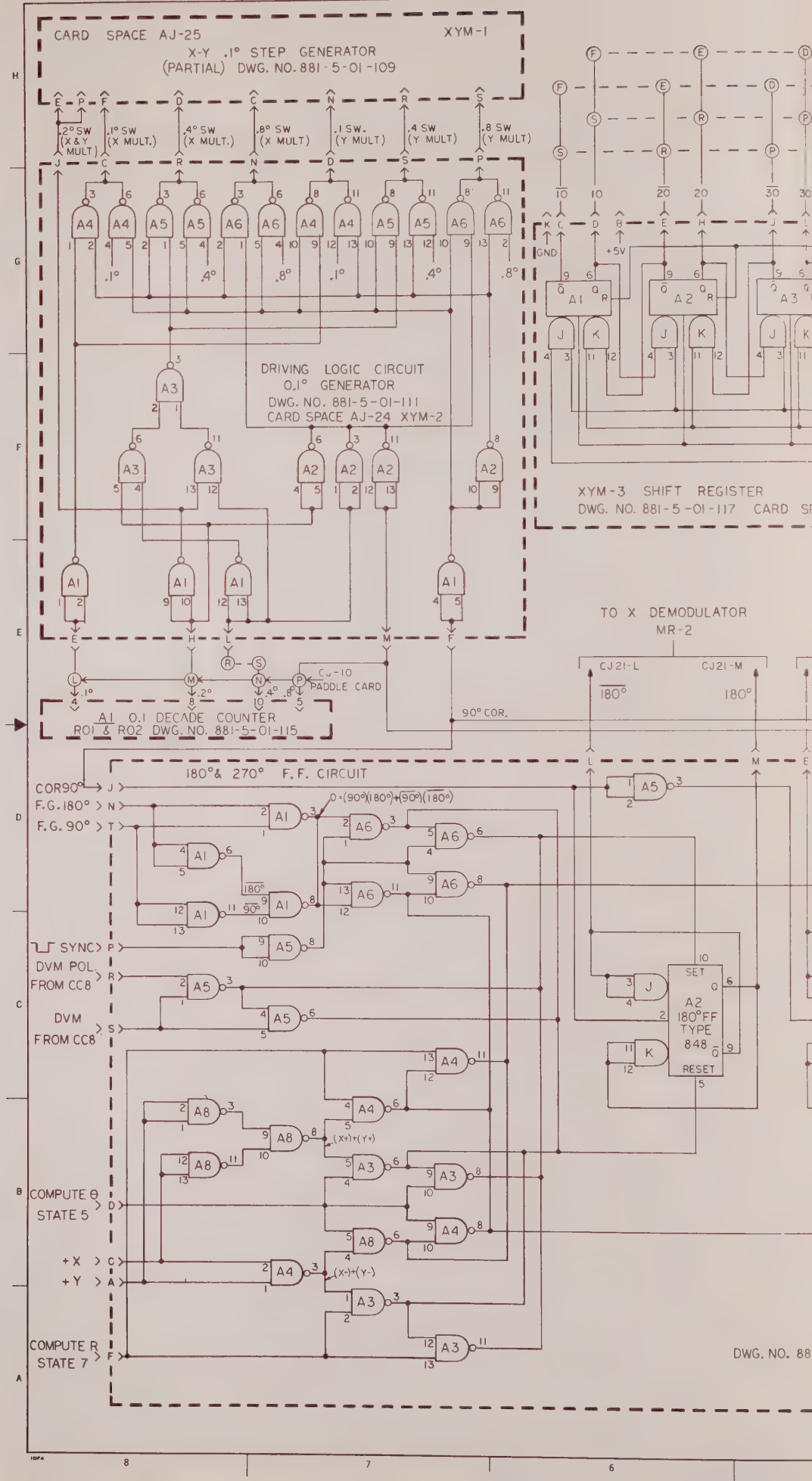
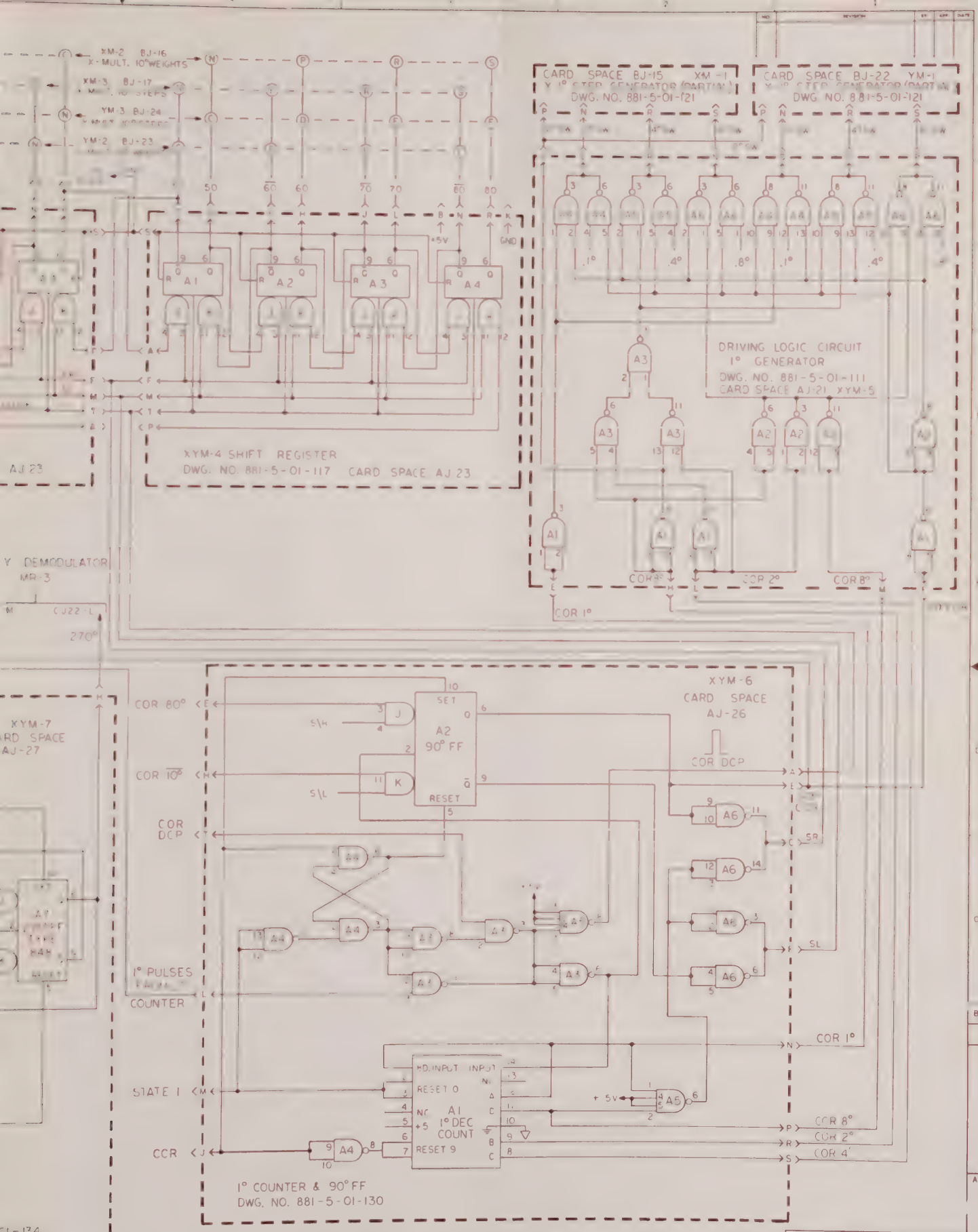
			DR E. BACHMAYER	THREE DEC PLCS ± .005 TWO DEC PLCS ± .010 FRACTIONS ± 1/64 ANGLES ± 0 30'		D 881-5-01-611 3
	DA1410		CHK			
NEXT ASSY	USED ON		APP			DWG SIZE / SCALE ~ / SHEET 1 OF 1 / DWG. REV.
APPLICATION			MATL	FINISH		

12 13 14 15 16 17 18 19 20 21


CARD SPACE AJ-25
XYM-1
X-Y .1° STEP GENERATOR
(PARTIAL) DWG. NO. 881-5-01-109
.2° SW (X & Y MULT)
.1° SW (X MULT.)
.4° SW (X MULT.)
.8° SW (X MULT)
.1 SW. (Y MULT)
.4 SW (Y MULT)
.8 SW (Y MULT)
DRIVING LOGIC CIRCUIT
0.1° GENERATOR
DWG. NO. 881-5-01-111
CARD SPACE AJ-24 XYM-2
XYM-3 SHIFT REGISTER
DWG. NO. 881-5-01-117 CARD SP
TO X DEMODULATOR
MR-2
CJ21-L
CJ21-M
180°
180°
CJ-10
PADDLE CARD
A1 0.1 DECADE COUNTER
RO1 & RO2 DWG. NO. 881-5-01-115
90° COR.
180° & 270° F.F. CIRCUIT
COR90°
F.G. 180°
F.G. 90°
SYNC
DVM POL. FROM CC8
DVM FROM CC8
COMPUTE θ STATE 5
+X
+Y
COMPUTE R STATE 7
A2 180°FF TYPE 848
SET
RESET
DWG. NO. 88

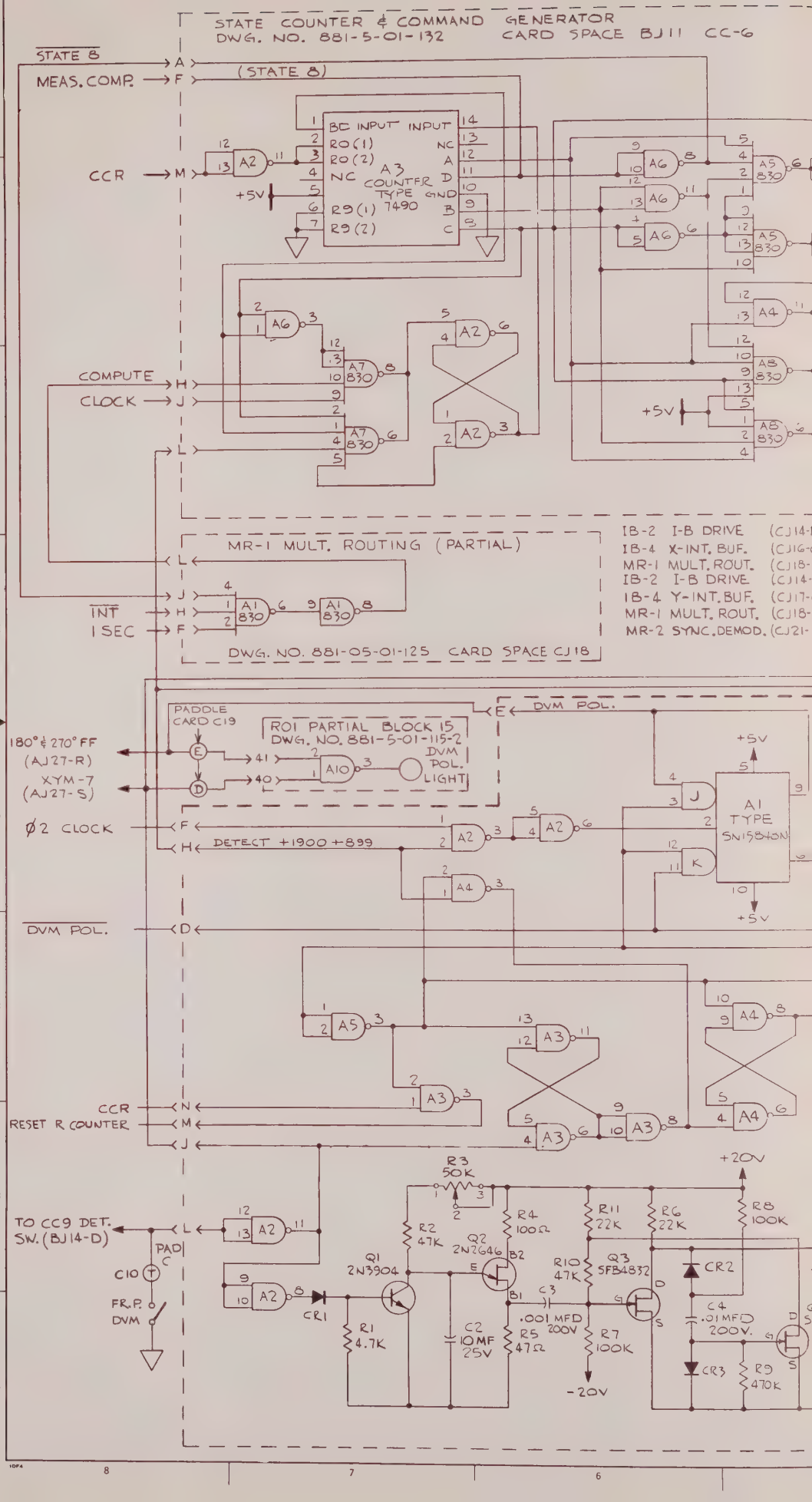


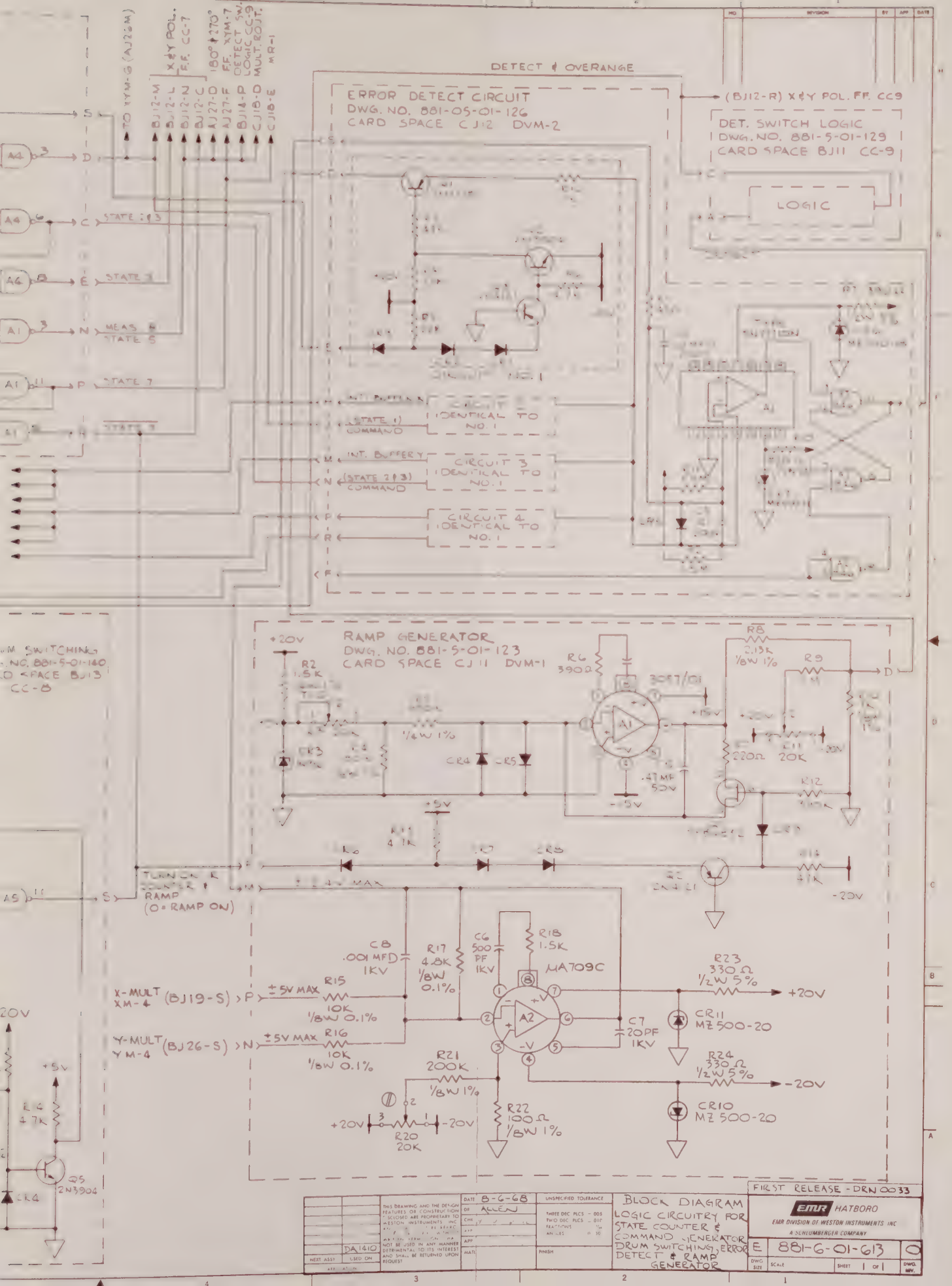
DRAWN	7-27-68	BLOCK DIAGRAM DRIVING AND LOGIC CIRCUITRY FOR X&Y MULTIPLIERS & X&Y DEMODULATORS	FIRST RELEASE · DRN 00312
DESIGNED	C.P.ALLEN		EMR HATBORO — EMR DIVISION OF WESTON INSTRUMENTS INC — A SCHLUMBERGER COMPANY
			E 881-6-01-612 0
			DWG SIZE — SCALE — SHEET 1 OF 1 — DWG. REV.

THIS DRAWING AND THE DESIGN FEATURES OF CONSTRUCTION ... AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT ... AND SHALL BE RETURNED UPON REQUEST.

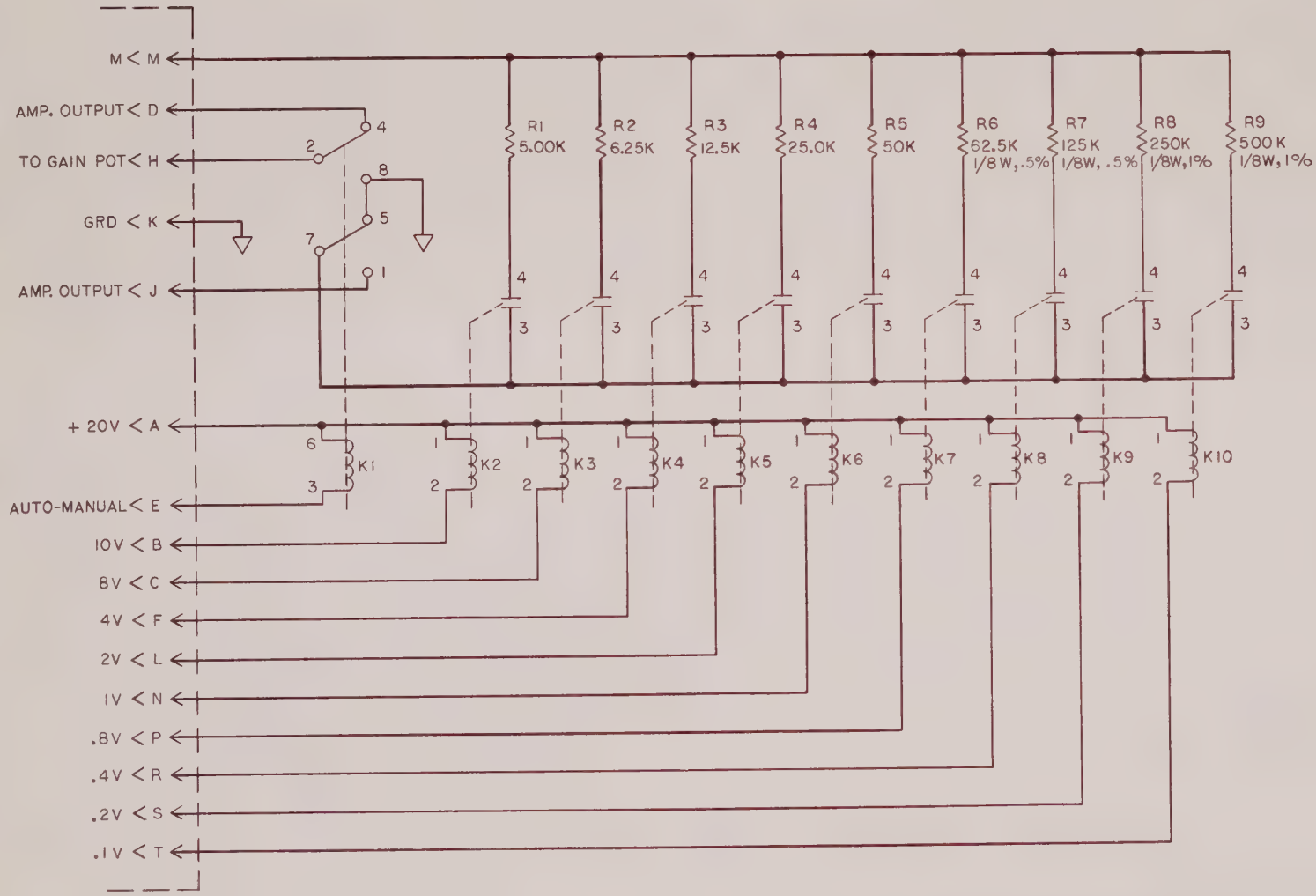
INSPECTED TOLERANCE: THREE DEC PLCS ± .005; TWO DEC PLCS ± .01; FRACTIONS ±; ANGLES ± 30'

NEXT ASSY | USED ON | APPLICATION


STATE COUNTER & COMMAND GENERATOR
DWG. NO. 881-5-01-132 CARD SPACE BJ11 CC-6
STATE 8
MEAS. COMP.
(STATE 8)
CCR
+5V
A3 COUNTER TYPE 7490
COMPUTE
CLOCK
MR-1 MULT. ROUTING (PARTIAL)
INT
1 SEC
DWG. NO. 881-05-01-125 CARD SPACE CJ18
IB-2 I-B DRIVE (CJ14-
IB-4 X-INT. BUF. (CJ16-
MR-1 MULT. ROUT. (CJ18-
IB-2 I-B DRIVE (CJ14-
IB-4 Y-INT. BUF. (CJ17-
MR-1 MULT. ROUT. (CJ18-
MR-2 SYNC. DEMOD. (CJ21-
PADDLE CARD C19
ROI PARTIAL BLOCK 15
DWG. NO. 881-5-01-115-2
DVM POL. LIGHT
DVM POL.
180° & 270° FF (AJ27-R)
XYM-7 (AJ27-S)
Ø2 CLOCK
DETECT +1900 +899
A1 TYPE SN7584N
CCR
RESET R COUNTER
TO CC9 DET. SW. (BJ14-D)
PAD C
C10
FR.P. DVM
CR1
Q1 2N3904
Q2 2N2646
Q3 SFB4832
R1 4.7K
R2 47K
R3 50K
R4 100Ω
R5 47Ω
R7 100K
R8 100K
R10 47K
R11 22K
R6 22K
C2 10MF 25V
C3 .001 MFD 200V
C4 .01 MFD 200V
CR2
CR3
R9 470K
+20V
-20V


DETECT & OVERANGE
ERROR DETECT CIRCUIT
DWG. NO. 881-05-01-126
CARD SPACE CJ12 DVM-2
DET. SWITCH LOGIC
DWG. NO. 881-5-01-129
CARD SPACE BJ11 CC-9
LOGIC
(BJ12-R) X&Y POL. FF. CC9
TO XYM-6 (AJ28-M)
X&Y POL. F.F. CC-7
180°±270° F.F. XYM-7 DETECT SW. LOGIC CC-9 MULT. ADJT. MR-1
BJ12-M
BJ12-L
BJ12-N
BJ12-C
AJ27-D
AJ27-F
BJ14-P
CJ18-D
CJ18-E
STATE 2&3
STATE 3
MEAS & STATE 5
STATE 7
STATE 9
INT. BUFFER
(STATE 1) COMMAND
CIRCUIT 2 IDENTICAL TO NO. 1
(STATE 2&3) COMMAND
CIRCUIT 3 IDENTICAL TO NO. 1
CIRCUIT 4 IDENTICAL TO NO. 1
CIRCUIT NO. 1
RAMP GENERATOR
DWG. NO. 881-5-01-123
CARD SPACE CJ11 DVM-1
+20V
-20V
+5V
-5V
R2 1.5K
R6 390Ω
R8 2.13K 1/8W 1%
R9
R11 20K
220Ω
R12
R13 4.7K
R14 4.7K
R1 4.99K 1/4W 1%
CR4
CR5
CR3
CR7
CR8
CR9
.47 MF 50V
TURN ON R COUNTER & RAMP (0 = RAMP ON)
+ 2.4V MAX
C8 .001 MFD 1KV
R17 4.8K 1/8W 0.1%
C6 500 PF 1KV
R18 1.5K
MA709C
A2
X-MULT XM-4 (BJ19-S)
Y-MULT YM-4 (BJ26-S)
±5V MAX
R15 10K 1/8W 0.1%
R16 10K 1/8W 0.1%
R21 200K 1/8W 1%
R20 20K
R22 100Ω 1/8W 1%
C7 20PF 1KV
R23 330Ω 1/2W 5%
R24 330Ω 1/2W 5%
CR11 MZ 500-20
CR10 MZ 500-20
Q5 2N3904
CR4
BLOCK DIAGRAM LOGIC CIRCUITRY FOR STATE COUNTER & COMMAND GENERATOR DRUM SWITCHING, ERROR DETECT & RAMP GENERATOR
FIRST RELEASE - DRN 0033
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY
881-6-01-613
DATE 8-6-68
DR ALLEN
DA1410

NO	REVISION	BY	CHK	APP	DATE
1	PRODUCTION RELEASE MARCH 15 1968 CPA				



NOTES:

1-UNLESS OTHERWISE SPECIFIED:
RESISTORS - 1/8W, 0.1%.
RELAYS - K1-TYPE 3118L
K2 THRU K10-TYPE 766068

NEXT ASSY	USED ON	
	DA1410	
APPLICATION		

THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION. SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST

DATE 12-23-67
DR. KEN CONTE
CHK
APP
APP
MATL.

UNSPECIFIED TOLERANCE
THREE DEC PLCS ±.005
TWO DEC PLCS ±.010
FRACTIONS ±1/64
ANGLES ±0°30'
FINISH

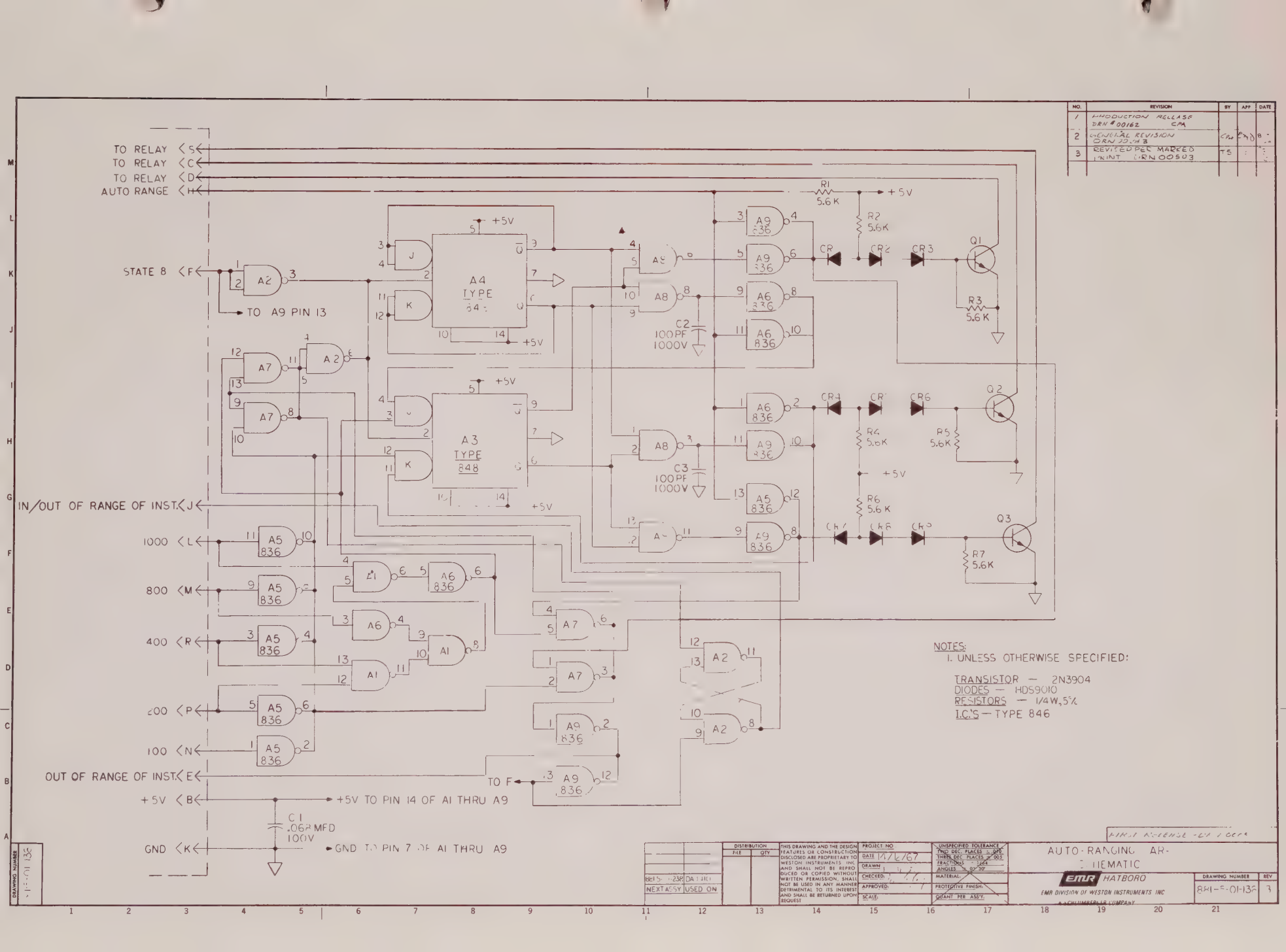
REMOTE AMPLITUDE PROGRAMMING OA-1 SCHEMATIC

FIRST RELEASE - DRN 00081

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

D | 881-5-01-108 | 1

DWG SIZE | SCALE | SHEET 1 OF 1 | DWG REV



NO.	REVISION	BY	APP	DATE
1	PRODUCTION RELEASE DRN # 00162 CM			
2	GENERAL REVISION DRN 00503 B	CM	[illegible]	8 - [illegible]
3	REVISED PER MARKED PRINT DRN 00503	TS		

DISTRIBUTION	FILE	QTY

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PROJECT NO	
DATE	11/6/67
DRAWN	
CHECKED	
APPROVED	
SCALE:	

UNSPECIFIED TOLERANCE
TWO DEC. PLACES ± .010
THREE DEC. PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0° 30'
MATERIAL:
PROTECTIVE FINISH:
GRAIN PER ASSY:

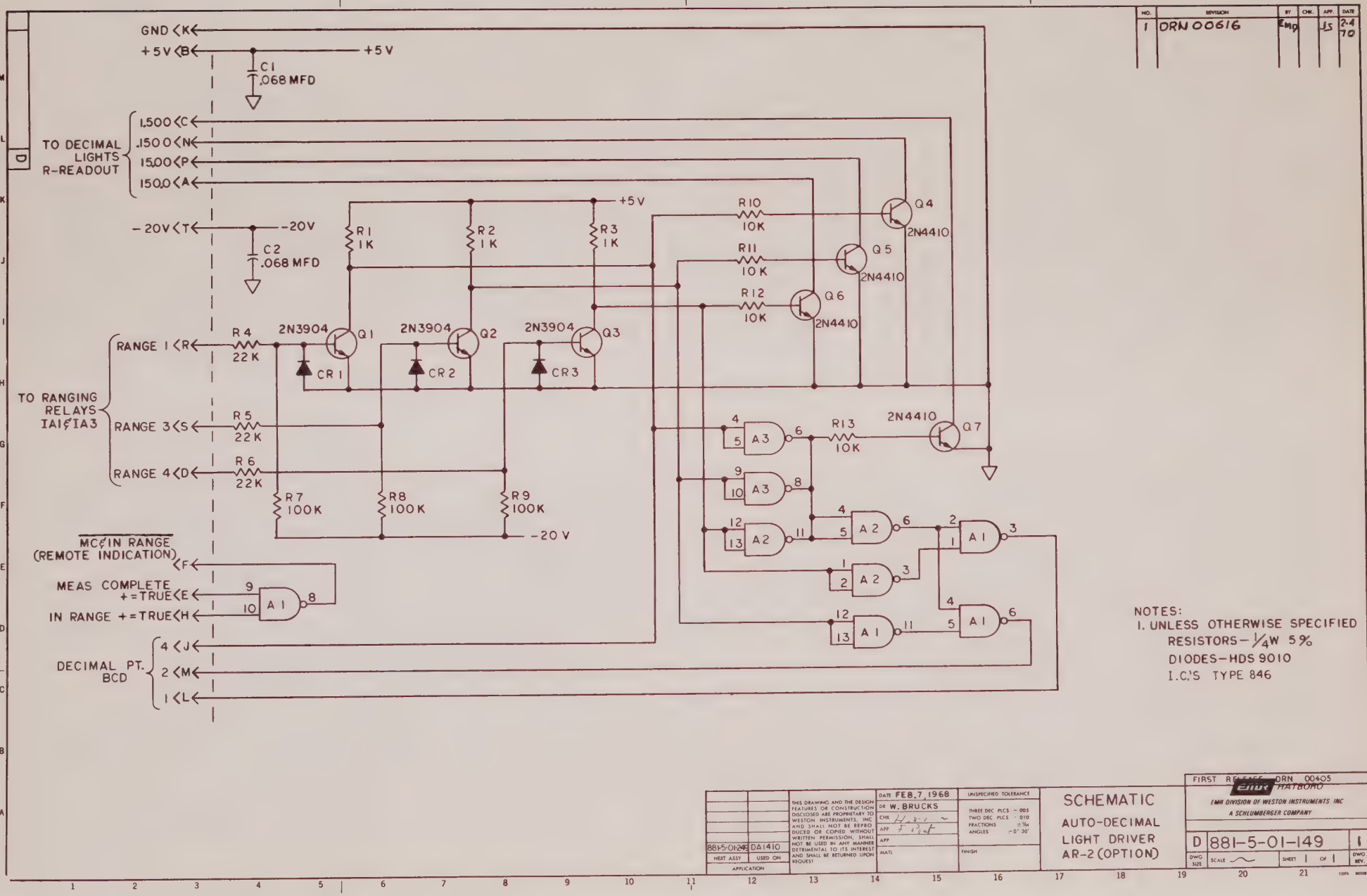
NEXT ASSY USED ON

AUTO-RANGING AR-
-TIEMATIC

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

DRAWING NUMBER 8M1-E-01-135 REV 3

DRAWING NUMBER 8M1-E-01-135



NO.	REVISION	BY	CHK.	APP.	DATE
1	DRN 00616	Emp		JS	2-4 70

NOTES:
1. UNLESS OTHERWISE SPECIFIED
RESISTORS – 1/4W 5%
DIODES – HDS 9010
I.C.'S TYPE 846

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DATE	FEB. 7, 1968
DR	W. BRUCKS
CHK	
APP	
APP	
MATL	
FINISH	

UNSPECIFIED TOLERANCE
THREE DEC PLCS – 005
TWO DEC PLCS – 010
FRACTIONS ±1/64
ANGLES – 0° 30'

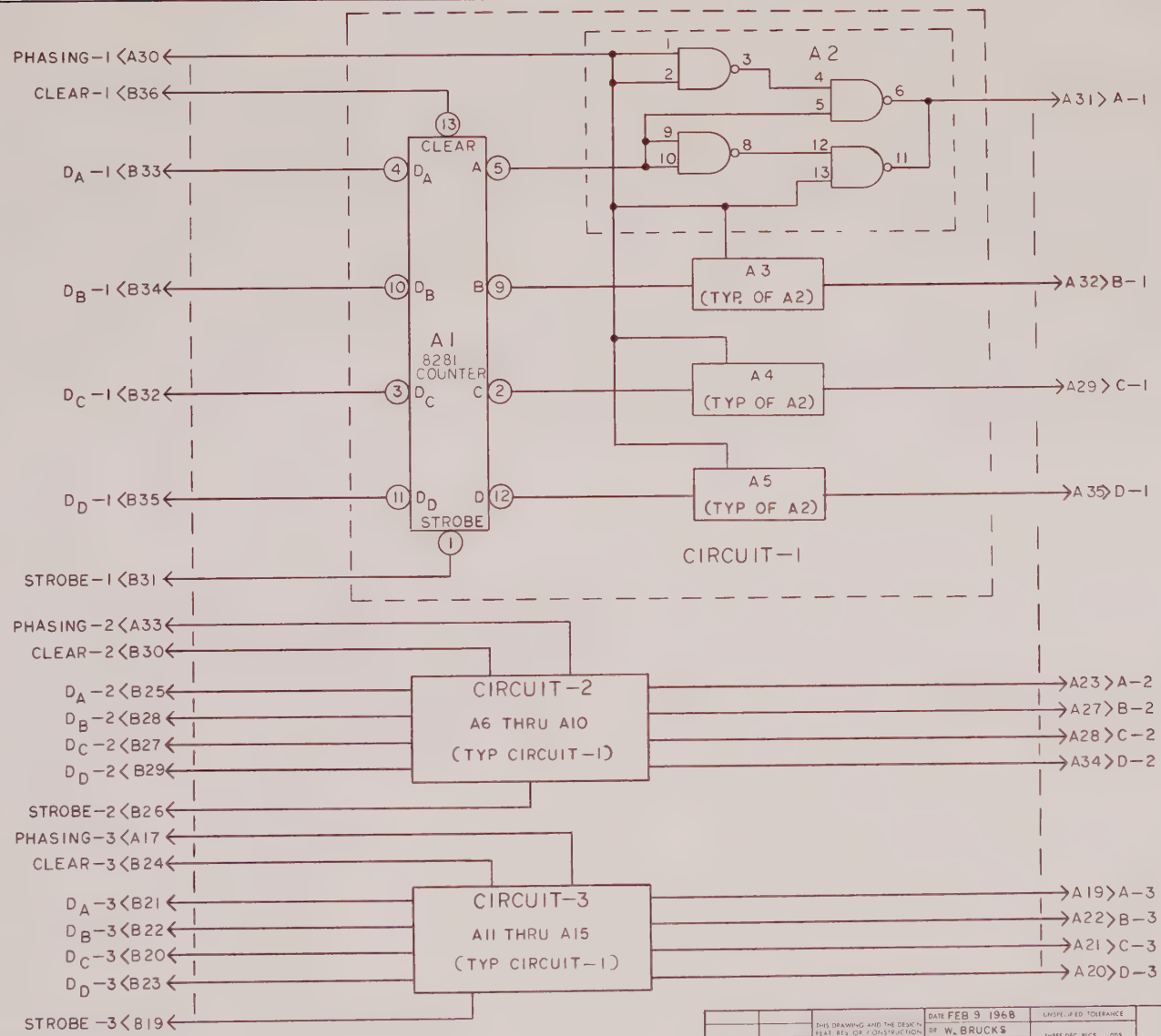
8815-01-245 DA1410
NEXT ASSY | USED ON
APPLICATION

SCHEMATIC
AUTO-DECIMAL LIGHT DRIVER AR-2 (OPTION)

FIRST RELEASE DRN 00405

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D | 881-5-01-149 | 1
DWG SIZE | SCALE | SHEET 1 OF 1 | DWG REV.



NOTES
1 UNLESS OTHERWISE SPECIFIED
I.C.'S - TYPE 846

NO.	REVISION	BY	CHK.	APP	DATE

FIRST RELEASE - DRN 00405

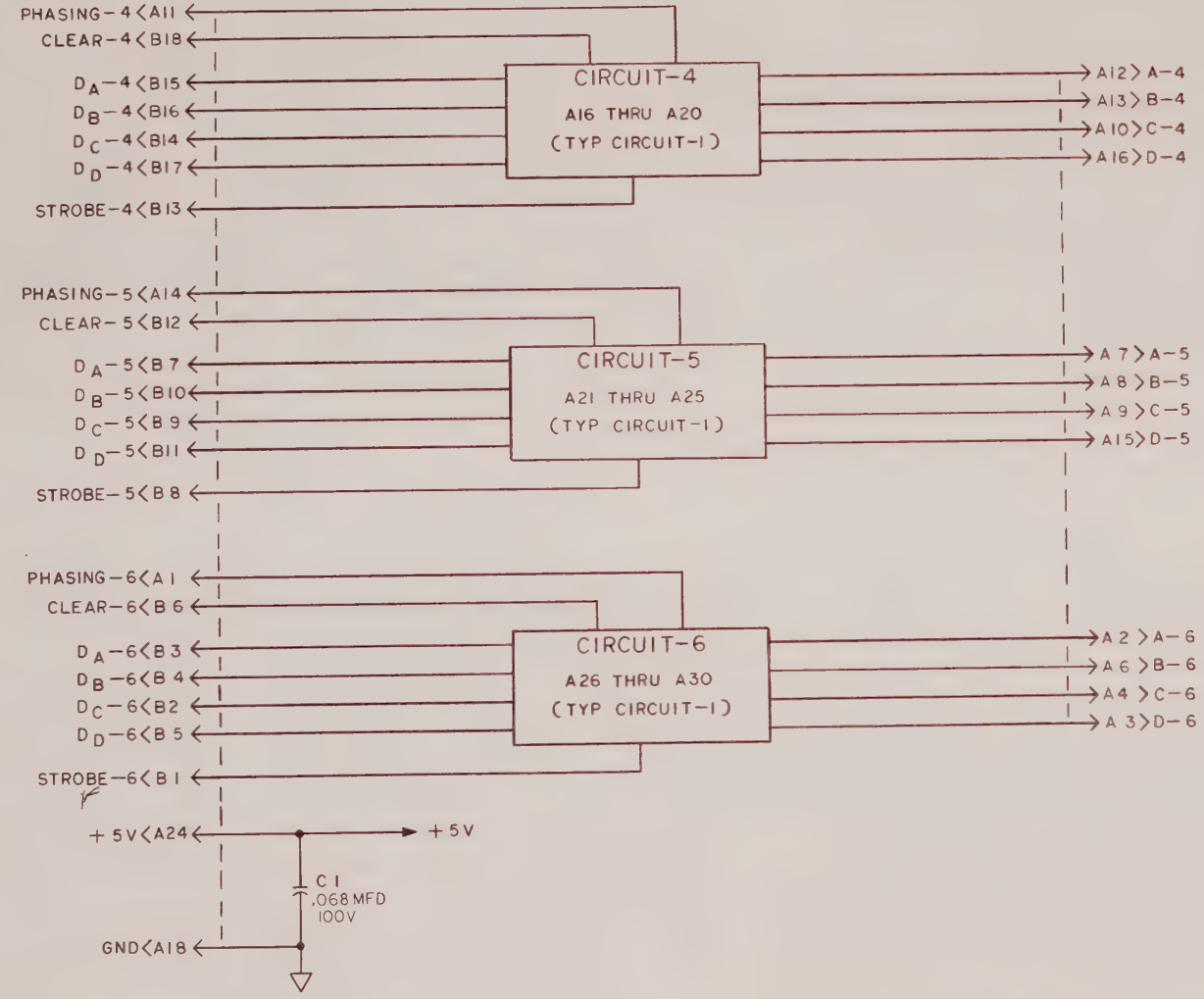
DATE FEB 9 1968
DR W. BRUCKS

SCHEMATIC
INPUT, OUTPUT
INTERFACE REMOTE
CONTROL MODULE

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D | 881-5-01-150 | 0

SHEET 1 OF 2



NO	REVISION	BY	CHK	APP.	DATE

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DATE FEB. 9, 1968
DR W. BRUCKS
CHK
APP.
APP
MATL

UNSPECIFIED TOLERANCE
THREE DEC PLCS ± .005
TWO DEC PLCS ± .010
FRACTIONS ± 1/64
ANGLES ± 0°30'

FINISH

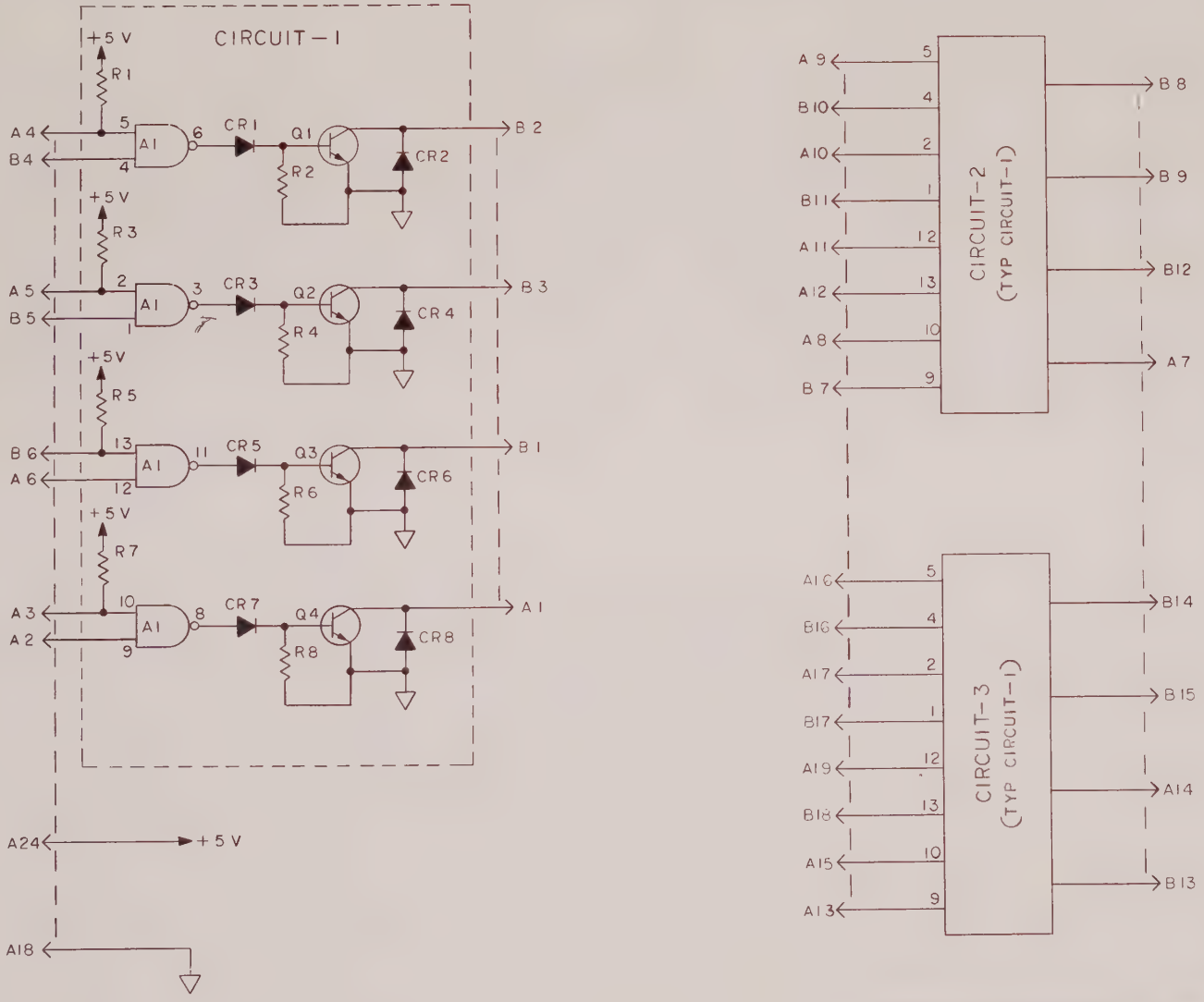
NEXT ASSY | USED ON
APPLICATION

SCHEMATIC INPUT, OUTPUT INTERFACE REMOTE CONTROL MODULE

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D 881-5-01-150 0

DWG SIZE | SCALE | SHEET 2 OF 2 | DWG REV



NO	REVISION	BY	APP.	DATE

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS, 4.7K ¼ W, 5%
   ALL DIODES, HDS 9010
   ALL TRANSISTORS, NPN
   2N3569
   ALL I.C.'S, TYPE 846

FIRST RELEASE —DRN 00405

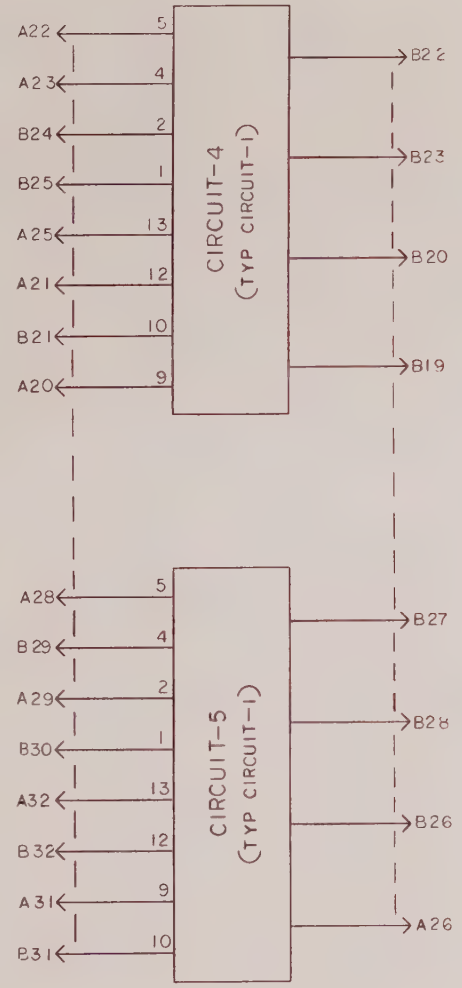
DISTRIBUTION		THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS INC AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION, SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST	PROJECT NO	UNSPECIFIED TOLERANCE
FILE	QTY		DATE FEB 16 1968	TWO DEC PLACES ± .010 THREE DEC PLACES ± .005 FRACTIONS ± 1/64 ANGLES ± 0° 30'
			DRAWN W BRUCKS	MATERIAL
			CHECKED	PROTECTIVE FINISH
			APPROVED	
			SCALE	QUANT PER ASSY

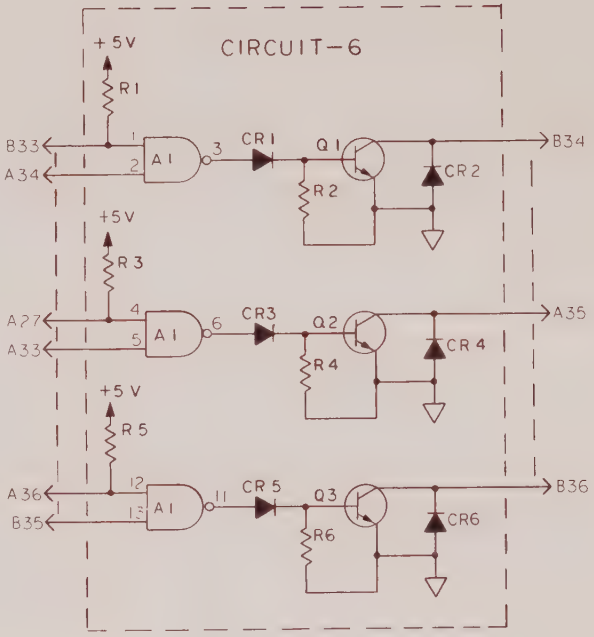
SCHEMATIC
GATED RELAY/LAMP DRIVER

EMR HATBORO
MR DIVISION OF WESTON INSTRUMENTS INC

DRAWING NUMBER 881-5-01-151 SHEET 1 OF 2 REV. 0

DRAWING NUMBER





NO.	REVISION	BY	APP.	DATE

DISTRIBUTION	
FILE	QTY

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PROJECT NO.:
DATE: FEB 16 1968
DRAWN: W BRUCKS
CHECKED:
APPROVED:
SCALE:

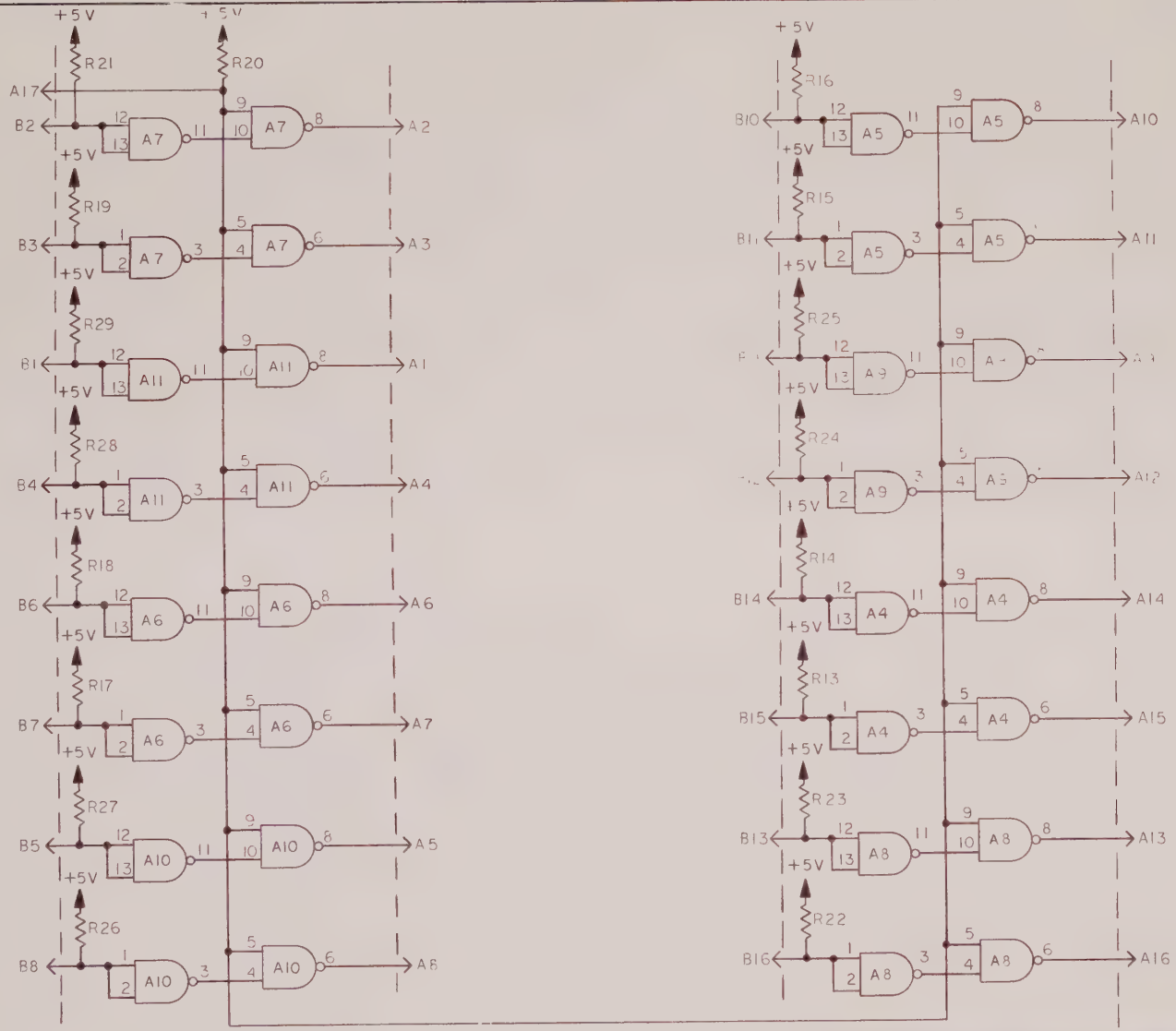
UNSPECIFIED TOLERANCE
TWO DEC. PLACES ± .010
THREE DEC. PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0° 30'
MATERIAL:
PROTECTIVE FINISH:
QUANT PER ASSY.

SCHEMATIC
GATED RELAY/ LAMP DRIVER

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC

DRAWING NUMBER: 881 5-01-151 SHEET 2OF2
REV: 0

DRAWING NUMBER



NOTE:
ALL RESISTORS ARE 4.7K, 1/4W, 5%.

NO.	REVISION	BY	APP.	DATE

FIRST RELEASE DRN # 00283

DISTRIBUTION	
FILE	QTY

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PROJECT NO.	0A1410
DATE:	2-19-68
DRAWN:	GOODFE...OW
CHECKED:	
APPROVED:	
SCALE	—H

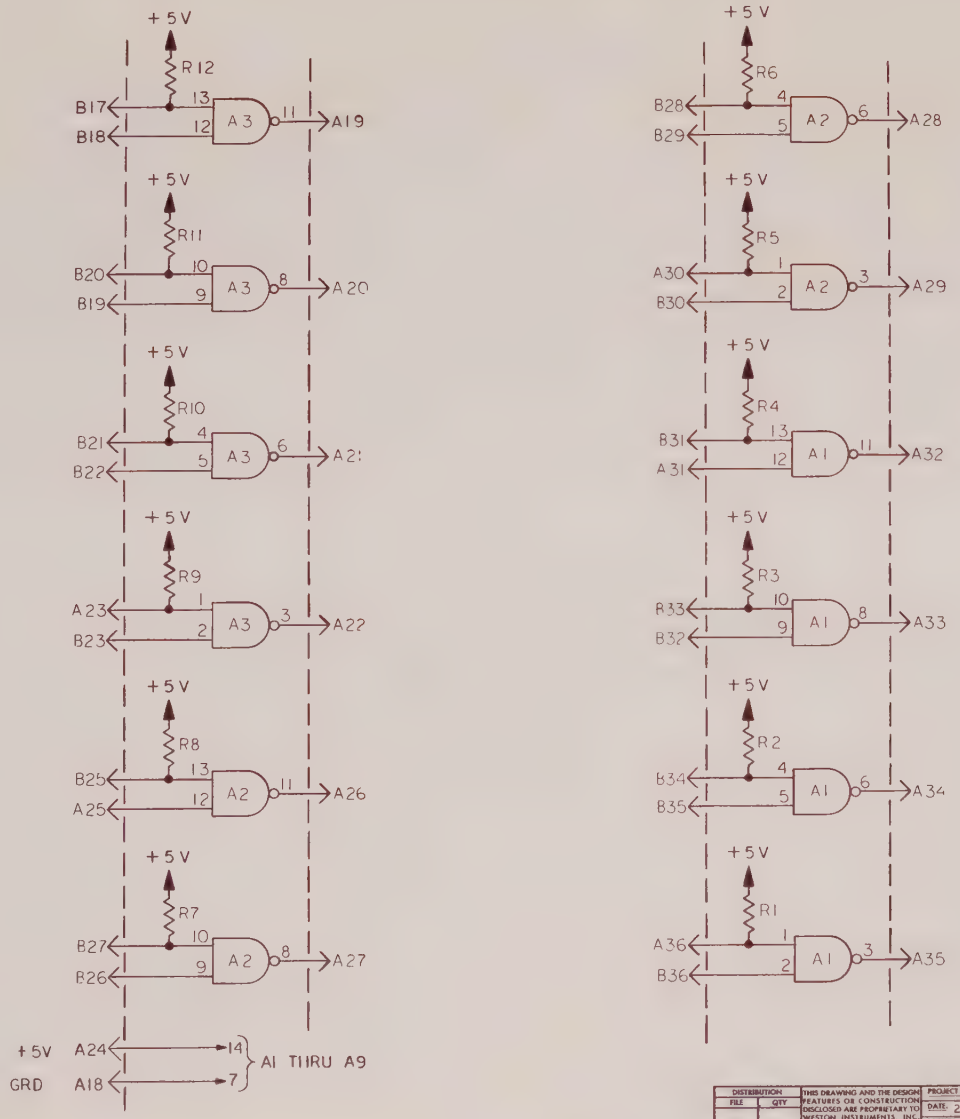
UNSPECIFIED TOLERANCE
TWO DEC. PLACES ± .010
THREE DEC. PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0° 30'
MATERIAL
PROTECTIVE FINISH:
QUANT PER ASS'Y

SCHEMATIC
MANUAL COMMAND BUFFERS

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC

DRAWING NUMBER: 881-5-01-152 SHT 1 OF 2
REV.

DRAWING NUMBER



NO.	REVISION	BY	APP.	DATE

FIRST RELEASE DRN # 00283

DISTRIBUTION	
FILE	QTY

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PROJECT NO. DA 1410
DATE: 2-19-68
DRAWN: GOOFELLOW
CHECKED:
APPROVED: EMD
SCALE: —

UNSPECIFIED TOLERANCE
TWO DEC. PLACES ± .010
THREE DEC. PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0° 30'
MATERIAL:
PROJECTIVE FINISH:
QUANT PER ASSY:

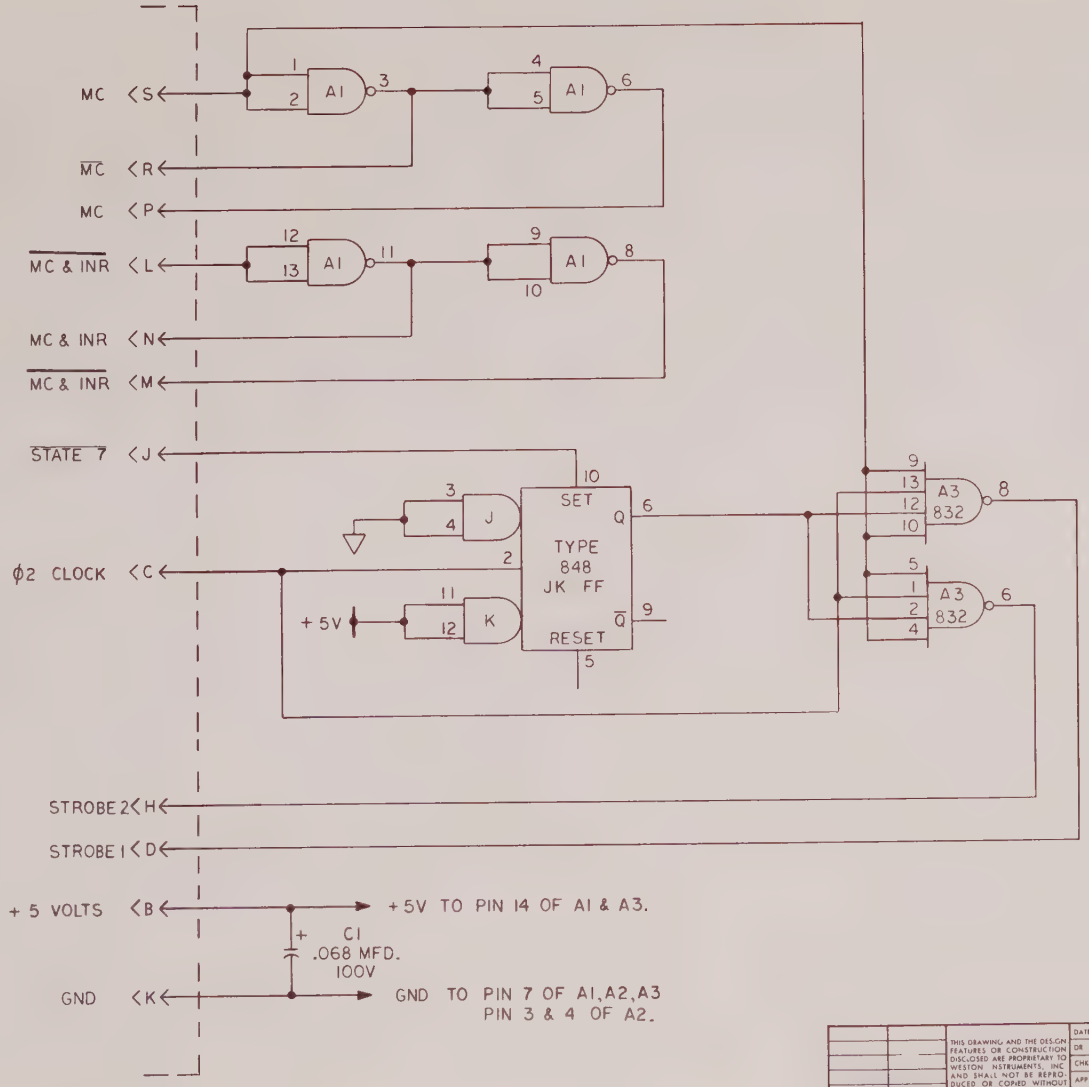
SCHEMATIC
MANUAL COMMAND BUFFERS

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC

DRAWING NUMBER: 881-5-01-152 SHT 2 OF 2
REV.: 0

DRAWING NUMBER

NO	REVISION	BY	CHK	APP	DATE
1	REVISED PIN TERMS L,M,N DRN 00616	EMO		JS	2/4/70



NOTES —
1. UNLESS OTHERWISE SPECIFIED:
I.C.'S TYPE 846.

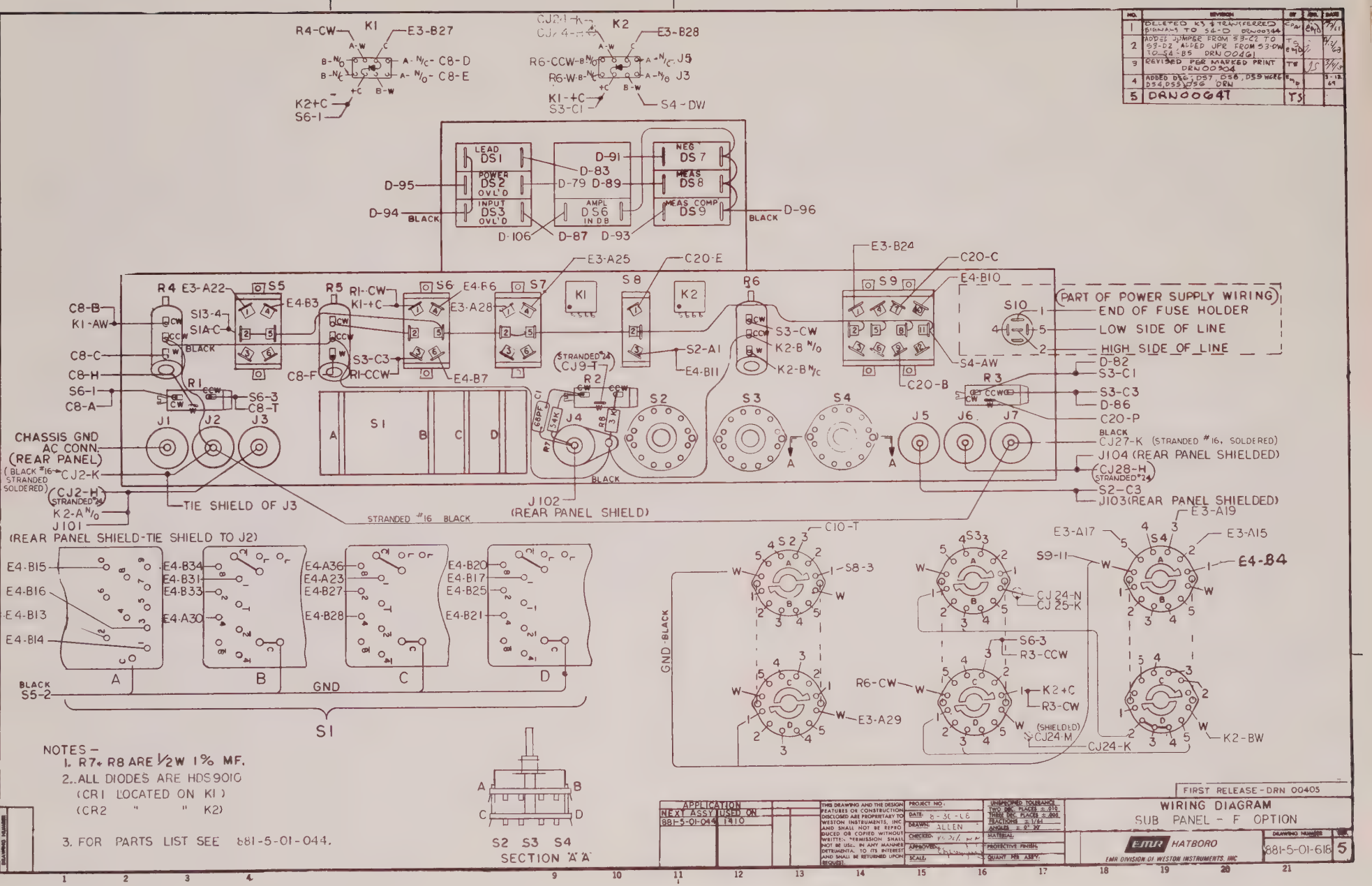
8815 0255 DA1410		THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC. AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION. SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST	DATE 6-28-68	UNSPECIFIED TOLERANCE	PRINTED WIRING BOARD STROBE CIRCUIT
NEXT ASSY	USED ON		DR ALLEN	THREE DEC PLCS ± .005 TWO DEC PLCS .010 FRACTIONS ±1/64 ANGLES 0° 30'	
APPLICATION			CHK		SCHEMATIC
			APP		
			APP		
			MATL	FINISH	

FIRST RELEASE — DRN 00344

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS INC
A SCHLUMBERGER COMPANY

D | 881-5-01-155 | 1

DWG SIZE | SCALE | SHEET 1 OF 1 | DWG REV



NO.	REVISION	BY	CHK.	DATE
1	DELETED K3 & TRANSFERRED SIGNALS TO S6-D DRN00344	CPM	BMB	7/11
2	ADDED JUMPER FROM S3-C2 TO S3-D2 ALSO UPD FROM S3-DW TO S4-B5 DRN 00461	CPM	BMB	7/12/68
3	REVISED PER MARKED PRINT DRN 00504	TS	JS	7/15/68
4	ADDED DS6, DS7, DS8, DS9 WIRES D54, D55, D56 DRN	CPM		3-12-69
5	DRN00641	TS		

FIRST RELEASE - DRN 00405

APPLICATION			
NEXT ASSY USED ON			
881-5-01-044	1410		

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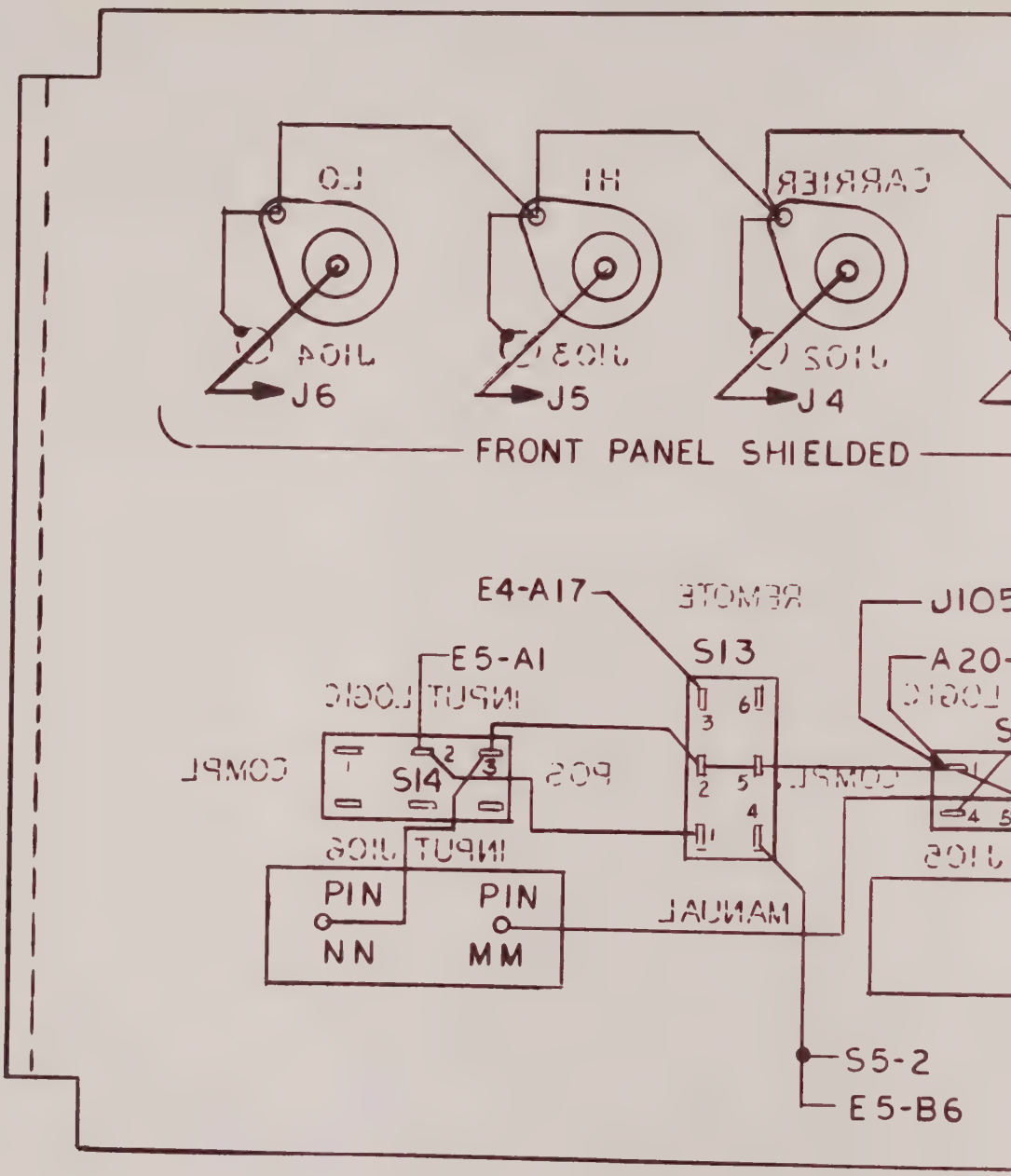
PROJECT NO.	
DATE	8-30-68
DRAWN	ALLEN
CHECKED	
APPROVED	
SCALE	

UNDIMENSIONED TOLERANCE
TWO DEC. PLACES ± .010
THREE DEC. PLACES ± .005
FRACTIONS ± 1/64
ANGLES ± 0° 30'
MATERIAL
PROTECTIVE FINISH
QUANT PER ASSY.

WIRING DIAGRAM
SUB PANEL - F OPTION

EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC

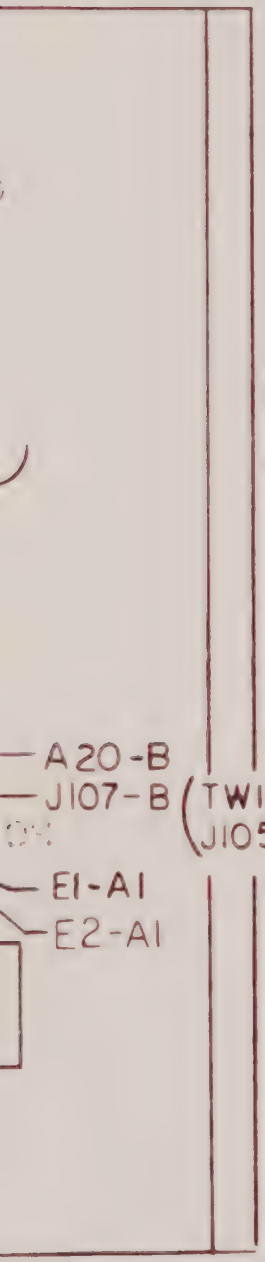
DRAWING NUMBER 881-5-01-618 5



B

		THIS DRAWING AND THE DESIGN FEATURES OR CONSTRUCTION DISCLOSED ARE PROPRIETARY TO WESTON INSTRUMENTS, INC. AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT WRITTEN PERMISSION, SHALL NOT BE USED IN ANY MANNER DETRIMENTAL TO ITS INTEREST AND SHALL BE RETURNED UPON REQUEST.	DATE 8-28-68	UNSPECIFIED TOLERA
			DR. ALLEN	
			CHK. [illegible]	THREE DEC. PLCS. ±.0
			APP. [signature]	TWO DEC. PLCS. ±.0
			APP.	FRACTIONS ±
881-4-01-063	DA 1410			ANGLES ±0°.
NEXT ASSY.	USED ON		MATL.	FINISH
APPLICATION				

NO.	REVISION	BY	CHK.	APP.	DATE
1	REVISED PER MARKED PRINT DRN# 00427	W.H.R.		EMD	11-13
2	ADDED J105-NN TO S12 DRN 00461	TS	EMD	[illegible]	12-20-68
3	ADDED J107-B AND RELATED NOTE DRN# 00553	TS	EMD	DEK	6/3/69



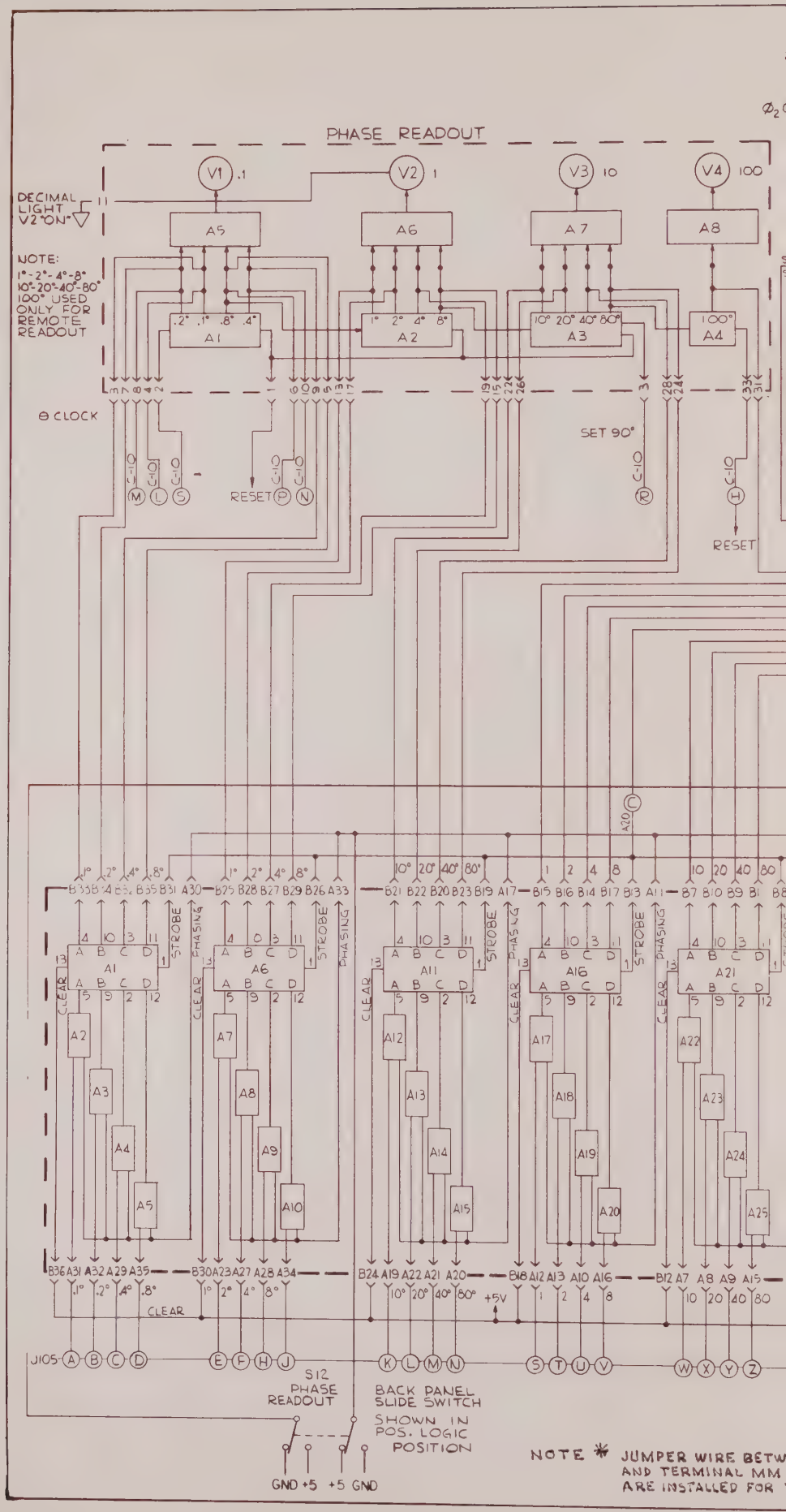
NOTE—
FOR ASSEMBLY SEE DWG. NO. 881-4-01-063.

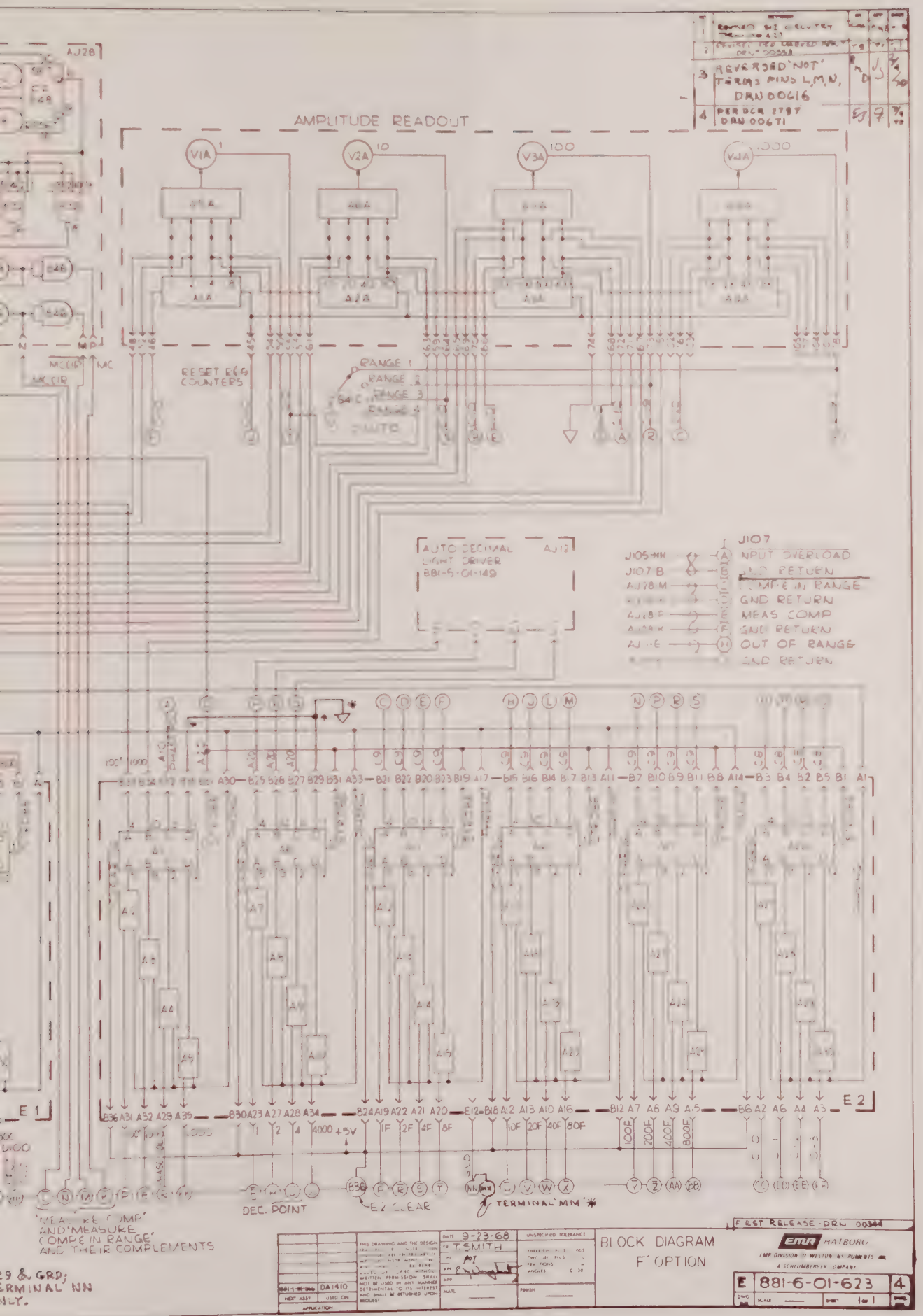
FIRST RELEASE — DRN. 00344

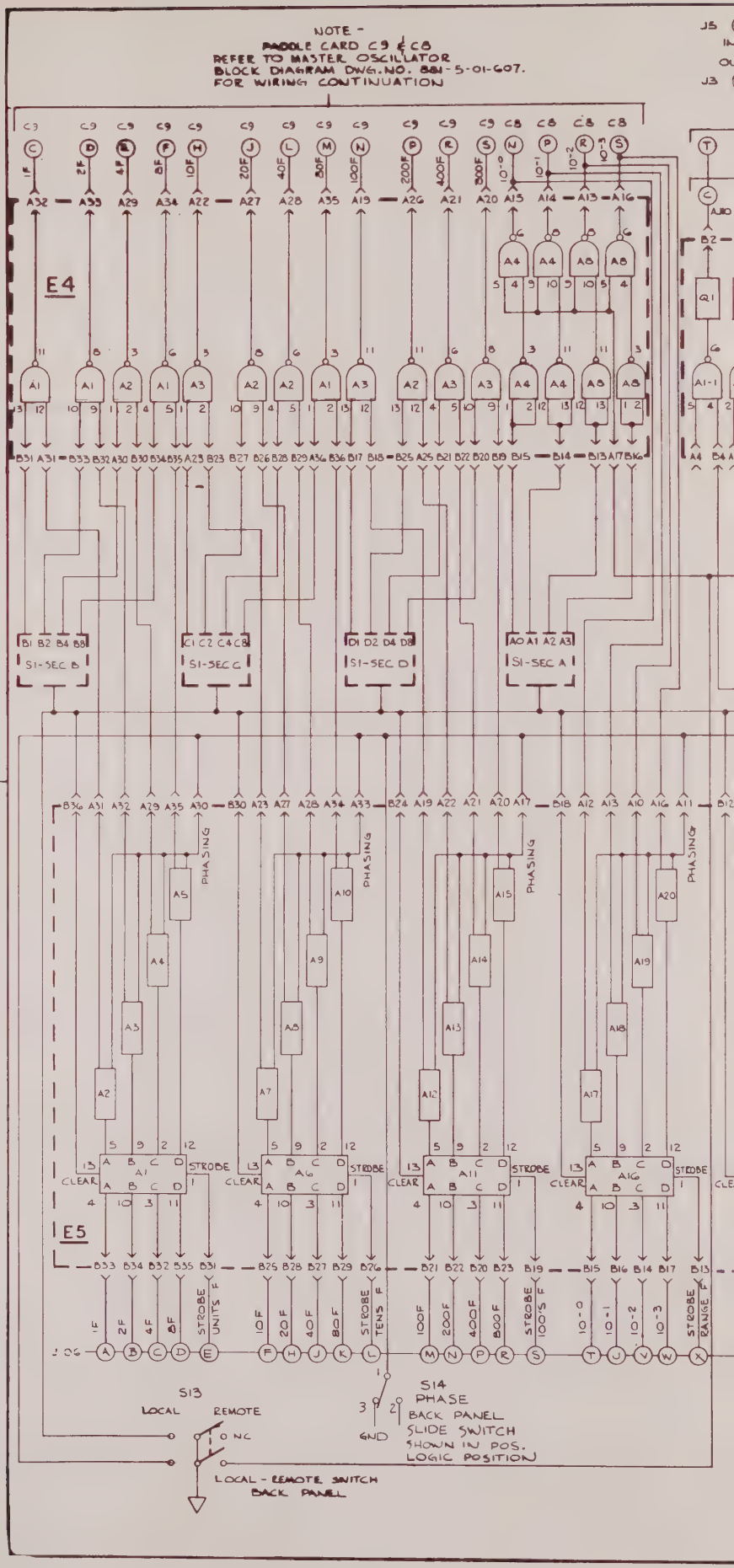
WIRING DIAGRAM
REAR PANEL
"F" OPTION

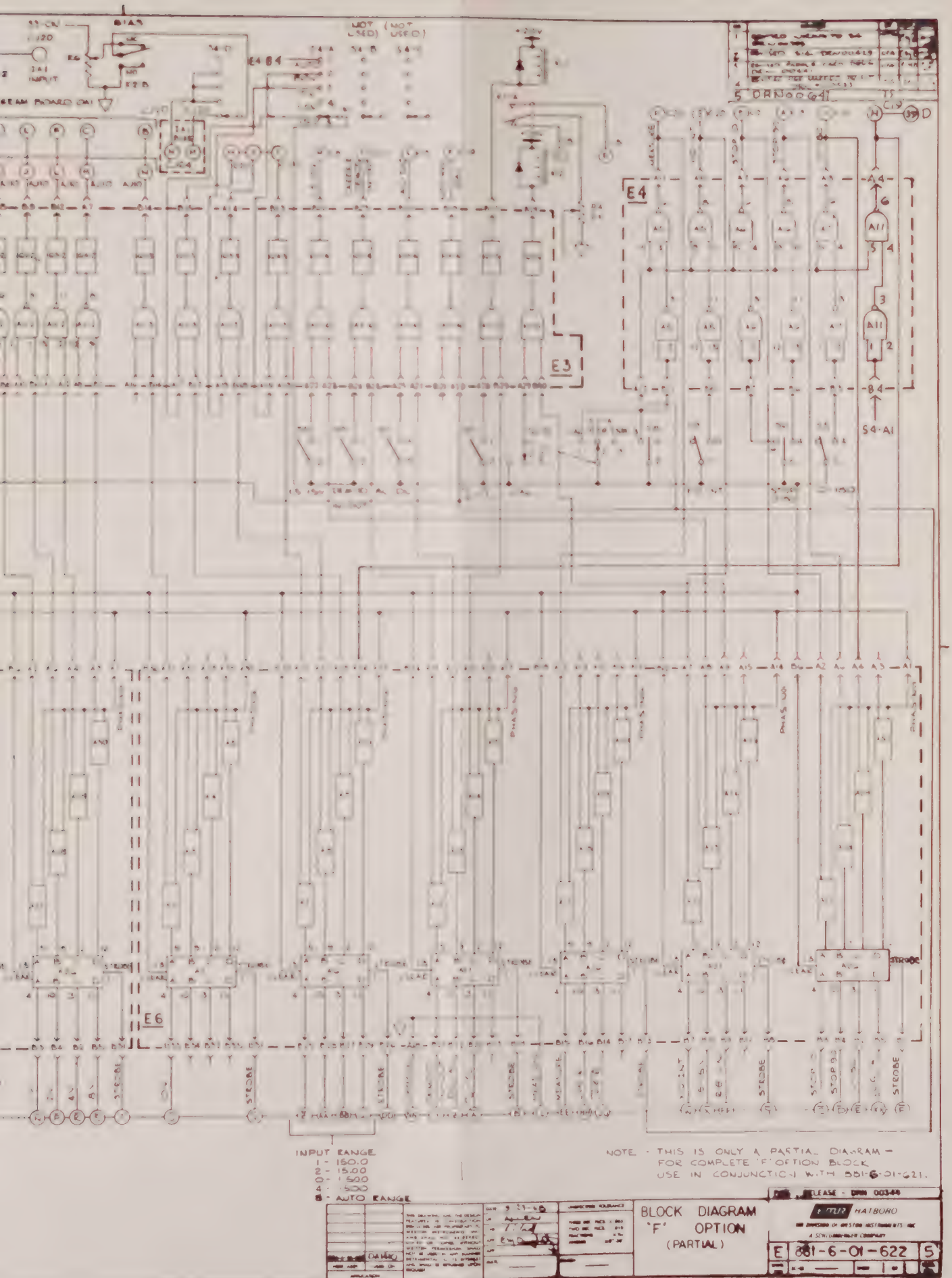
EMR HATBORO
EMR DIVISION OF WESTON INSTRUMENTS, INC
A SCHLUMBERGER COMPANY

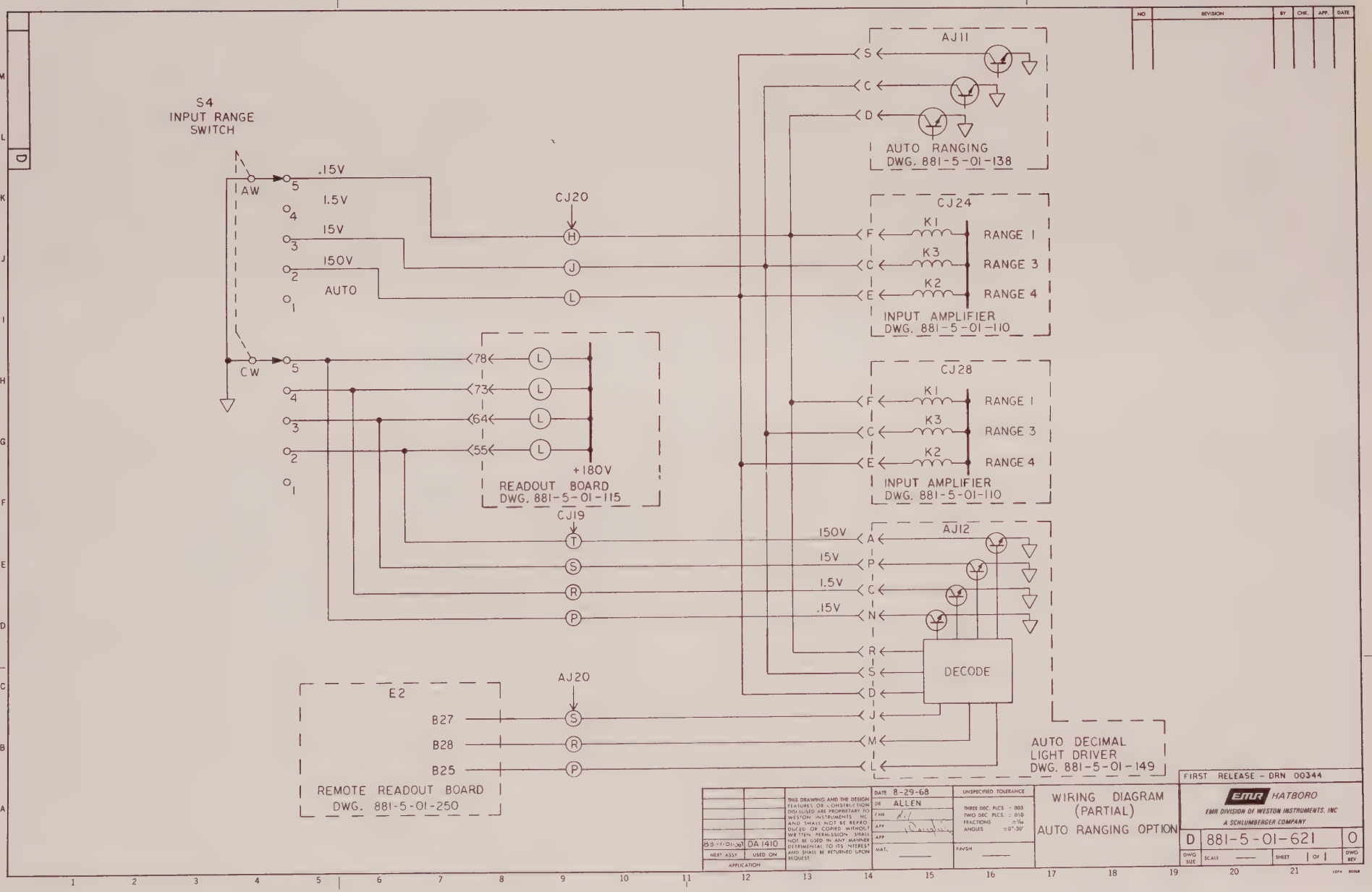
B	881-3-01-616	3
DWG. SIZE	SCALE —— SHEET 1 OF 1	DWG. REV.


PHASE READOUT
V1 .1
V2 1
V3 10
V4 100
DECIMAL LIGHT V2 "ON"
NOTE:
1°-2°-4°-8°
10°-20°-40°-80°
100° USED ONLY FOR REMOTE READOUT
A5
A6
A7
A8
A1
A2
A3
A4
Θ CLOCK
SET 90°
RESET
STROBE
PHASING
CLEAR
+5V
J105
S12 PHASE READOUT
BACK PANEL SLIDE SWITCH
SHOWN IN POS. LOGIC POSITION
GND +5 +5 GND
NOTE * JUMPER WIRE BETW
AND TERMINAL MM
ARE INSTALLED FOR


AMPLITUDE READOUT
V1A 1
V2A 10
V3A 100
V4A 1000
RESET E&G COUNTERS
RANGE 1
RANGE 2
RANGE 3
RANGE 4
AUTO
S4
AUTO DECIMAL LIGHT DRIVER 881-5-01-149
AJ12
J107
INPUT OVERLOAD
GND RETURN
COMPEN RANGE
GND RETURN
MEAS COMP
GND RETURN
OUT OF RANGE
GND RETURN
E1
E2
DEC. POINT
E2 CLEAR
TERMINAL 'MM'
'MEASURE COMP' AND 'MEASURE COMPE IN RANGE' AND THEIR COMPLEMENTS
REVERSED 'NOT' TERMS PINS L,M,N, DRN 00616
PER DCR 2797 DRN 00671
BLOCK DIAGRAM F OPTION
FIRST RELEASE - DRN 00344
EMR HATBORO
A SCHLUMBERGER COMPANY
881-6-01-623
DATE 9-23-68
T. SMITH
DA1410


NOTE -
PADDLE CARD C9 & C8
REFER TO MASTER OSCILLATOR
BLOCK DIAGRAM DWG.NO. 881-5-01-607.
FOR WIRING CONTINUATION
E4
E5
S1-SEC B
S1-SEC C
S1-SEC D
S1-SEC A
PHASING
STROBE
CLEAR
S13
LOCAL
REMOTE
LOCAL - REMOTE SWITCH
BACK PANEL
S14
PHASE
BACK PANEL
SLIDE SWITCH
SHOWN IN POS.
LOGIC POSITION
GND


BIAS
(NOT USED)
(NOT USED)
E4
E3
E6
S4-A1
STROBE
INPUT RANGE
1 - 150.0
2 - 15.00
0 - 1.500
4 - .1500
8 - AUTO RANGE
NOTE - THIS IS ONLY A PARTIAL DIAGRAM - FOR COMPLETE 'F' OPTION BLOCK USE IN CONJUNCTION WITH 881-6-01-621.
BLOCK DIAGRAM
'F' OPTION
(PARTIAL)
HAIBORO
E
881-6-01-622
S



NO	REVISION	BY	CHK.	APP.	DATE

DATE 8-29-68	UNSPECIFIED TOLERANCE	WIRING DIAGRAM (PARTIAL)	FIRST RELEASE - DRN 00344
DR ALLEN	THREE DEC. PLCS. ± .005 TWO DEC. PLCS. ± .010 FRACTIONS ±1/64 ANGLES ±0°-30'	AUTO RANGING OPTION	EMR HATBORO EMR DIVISION OF WESTON INSTRUMENTS, INC A SCHLUMBERGER COMPANY
CHK			D 881-5-01-621 0
APP			DWG SIZE — SCALE — SHEET 1 OF 1 DWG REV
APP			
MAT. —	FINISH —		
83-11-01-30 DA 1410			
NEXT ASSY USED ON			
APPLICATION			

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7. REPLACEMENT PARTS

7.1 Introduction - The following subsections contain the information necessary to stock and order spare parts. Rather than list a recommended quantity for each part, the quantity shows the approximate number of parts used per instrument. This enables the purchaser to determine what percentage of spare parts he wishes to stock with respect to the degree of repair work he wishes to do.

7.2 Ordering Information - Address orders to EMR-Hatboro, County Line Road, Hatboro, Pennsylvania 19040.

7.2.1 Parts listed in spare parts list:

a. Part Number
b. Description of the part.

7.2.2 Parts not listed in spare parts list:

a. Instrument Model Number
b. Instrument Serial Number
c. Description of the Part
d. Location of the Part.

7.3 Spare Parts List

Quantity Used/Inst.	EMR Part Number	Description
4	010-3-09-001	Amplifier 111-5
2	-003	" 105
2	-004	" 141C
1	015-3-20-010	Capacitor 62pf 500v 10%
2	-042	" 1300pf " "
2	-043	" 39pf " "
2	-044	" 15pf " "
5	-045	" 100pf " "
2	015-3-53-002	" 9-35pf Trimmer
2	-003	" 15-60pf "
2	-004	" 2.5-11pf "
2	015-3-70-001	" 4.0 μf 100v 1%
1	-002	" .47 μf 50v
1	015-3-90-001	" 4700pf 50v NPO Ceramic
1	025-3-01-029	Diode 1N821 Zener
49	-062	" MZ500-20 "
2	-064	" MZ500-18 "
2	-065	" MZ500-11 "
4	-066	" 1N936 Reference
2	-067	" MZ500-16 Zener
2	-074	" MZ500-25 "

Quantity Used/Inst.	EMR Part Number	Description
115	025-3-04-004	Diode HDS9010
2	025-3-07-023	" 407B
1	025-3-12-002	" 1N4733A
22	025-3-15-001	" 384A
1	-002	" 384M
11	-003	" 384B
1	025-3-18-001	" 1N3716
3	025-3-19-001	" 2N4441
1	None	Fuse 1.5 Amp 115v operation
1	None	" .75 Amp 230v "
6	033-3-03-001	Indicator Light, Center of Diplay Area
6	035-3-10-003	Integrated Circuit Amp 709C To-5
9	-005	" " " 3057/01 "
2	-006	" " " 3056/01 "
34	035-3-11-001	" " Flip Flop SN15848N
81	-002	" " Nand Gate SN15846N
9	-003	" " " " SN15830N
2	-004	" " Extender SN15833N
3	-005	" " Nand Gate SN15832N
24	-006	" " Counter N8281A (F & P Option only)
2	-007	" " Comparator SN72710N
23	-013	" " Dec. Counter SN7490N
1	-016	" " Nand Gate SN15844N
8	035-3-12-001	" " Driver SN7441N
3	035-3-20-001	" " Regulator LM300
5	035-3-11-018	" " Hex Inverter MC 836P
2	038-3-06-001	Potentiometer 20K Series 274
1	-004	" 50K " "
6	038-3-15-001	" 2K 3007P-1-202
22	-002	" 20K 3007P-1-203
6	-003	" 5K 3007P-1-502
1	-005	" 10Ω 3007P-1-100
5	-006	" 1K 3007P-1-102
3	-007	" 500Ω 3007P-1-501
7	038-3-16-001	" 50K 79PR50K
1	038-3-17-001	" 2K 3507S-1-516-202
2	-002	" 5K 3507S-1-516-502
1	053-3-05-001	Transformer XT 109
3	054-3-01-014	Transistors 2N697
3	-042	" 40362
2	-044	" 40321
23	-045	" 2N3569 (F Option only)

Quantity Used/Inst.	EMR Part Number	Description
32	054-3-03-022	Transistors 2N4121
1	-025	" 2N2646
3	054-3-05-013	" 2N3232
2	054-3-07-003	" 2N2945
21	-004	" 2N3218
4	054-3-08-001	" 2N3819
27	-002	" 2N3904
26	-008	" SFB4832
10	-009	" 2N4410
1	054-3-11-002	" A604
68	054-3-19-001	" Fet Module (White)
4	-002	" " " (Black)
8	055-3-01-001	Readout Tube NL841
2	042-3-13-001	Relay RP 7633 622 (F Option only)

7.4 Printed Circuit Board List:

If it is more desirable to stock spare parts at the printed circuit board level, they may be ordered from the following list.

Quantity Used/Inst.	EMR Part Number	Description
1	881-5-01-200	PC Card OA-2
2	-201	PC Card IN-2 (Y), IN-1 (X)
1	-202	" " MO-3
2	-203	" " IB-4 (X), IB-5 (Y)
3	-205	" " XM-3, FG-2, YM-3
3	-206	" " YM-2, XM-2, FG-3
1	-207	" " IB-3
1	-209	" " XYM-1
2	-210	" " IA-1 (HI) & IA-3
2	-211	" " XYM-5, XYM-2
1	-214	" " FG-8
1	-215	" " Display
2	-216	" " MR-2 (X), MR-3
4	-217	" " FG-6, FG-7, XYM-3, XYM-4
1	-218	" " IB-2
1	-219	" " FG-9
1	-220	" " MO-2
3	-221	" " XM-1, YM-1, FG-4
1	-222	" " P.S.
1	-223	" " DVM-1
1	-224	" " FR-1
1	-225	" " MR-1

Quantity Used/Inst.	EMR Part Number	Description
1	881-5-01-226	PC Card DVM-2
1	-227	" " FG-5
1	-228	" " CC-7
1	-229	" " CC-9
1	-230	" " XYM-6
1	-231	" " CC-2
1	-232	" " CC-6
1	-233	" " CC-3
1	-234	" " XYM-7
1	-235	" " MO-1
1	-236	" " MO-4
1	-237	" " MO-5
1	-239	" " CC-4
1	-240	" " CC-8
1	-241	" " IA-2
1	-242	" " FG-1
1	-243	" " CC-5
1	-244	" " CC-1
2	-245	" " XM-4, YM-4
1	-247	" " 5V P. S.
1	-248	" " IA-4
1	-253	" " Extender

7.5 - SPARE PRINTED CIRCUIT BOARD LIST FOR OPTIONS AR AND F

Qty. Used/Instrument	Option	EMR Part No.	Description
1	F	881-5-01-208	Remote Amplitude Programming
1	AR, F	881-5-01-238	Auto-Ranging
1	AR, F	881-5-01-249	Auto-Decimal Drivers
4	F	881-5-01-250	In/Out Interface Remote Control
1	F	881-5-01-251	Gated Relay/Lamp Driver
1	F	881-5-01-252	Manual Command Buffers
1	F	881-5-01-255	Output Strobe

Quantity Used/Inst.	EMR Part Number	Description
1	881-5-01-226	PC Card DVM-2
1	-227	" " FG-5
1	-228	" " CC-7
1	-229	" " CC-9
1	-230	" " XYM-6
1	-231	" " CC-2
1	-232	" " CC-6
1	-233	" " CC-3
1	-234	" " XYM-7
1	-235	" " MO-1
1	-236	" " MO-4
1	-237	" " MO-5
1	-239	" " CC-4
1	-240	" " CC-8
1	-241	" " IA-2
1	-242	" " FG-1
1	-243	" " CC-5
1	-244	" " CC-1
2	-245	" " XM-4, YM-4
1	-247	" " 5V P. S.
1	-248	" " IA-4
1	-253	" " Extender

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1	AR, F	881-5-01-238	Auto-Ranging
1	AR, F	881-5-01-249	Auto-Decimal Drivers
4	F	881-5-01-250	In/Out Interface Remote Control
1	F	881-5-01-251	Gated Relay/Lamp Driver
1	F	881-5-01-252	Manual Command Buffers
1	F	881-5-01-255	Output Strobe

8 - APPENDIX

8.1 - Appendix A

MODEL 1410 COMPUTATIONAL THEORY

The 1410 performs a true Fourier Analysis on the return signal from a device under test with the source signal from the function generator serving as a phase reference. The correlator multiplies the return signal by sin ωt and cos ωt where ω is the frequency of the generator section. The multiplier outputs are then integrated over an integral number of cycles of the generated frequency. Thus, the output of the two integrators is proportional to the cartesian components of the Fourier Integral.

(1) Real Component = $\int_0^T X(t)\, A \cos \omega t \, dt$

Where: $X(t)$ = unknown signal = $R \sin(\omega t + \theta)$ and R = gain of device under test

θ = phase shift of device under test

A = Peak value of cos or sin multiplier

T = is made equal to an integral number of cycles

(2) Imaginary Component = $\int_0^T X(t)\, A \sin \omega t \, dt$

If the return signal, $X(t)$ is represented as R Sine $(\omega t + \theta)$ then the Cartesian coordinates just described compute to be R Sin θ and R cos θ the imaginary and real parts respectively from equations (1) and (2). After the initial Fourier integral computation is completed the instrument re-routes the fixed Cartesian results through a polar resolver.

The polar resolving technique uses the same multipliers that performed the Fourier integral. The Cartesian coordinates, stored in the two integrators, are fed to the two multipliers (Imaginary to Cos Multiplier and Real to Sin Multiplier). The sine and cos multipliers are then started at T = 0 (0° for sine and 90° for cos) and stepped through sequential phase values at a controlled rate. During this time the outputs of the two multipliers are as follows:

Cosine Multiplier output = R Sin θ Cos Y.

Where: Y is the running phase value of the multiplier.

At the same time the Sin multiplier output is:

$$\text{Sine Multiplier Output} = R \cos \theta \sin Y$$

The two multiplier outputs are compared as Y (phase) is allowed to run, and the process is stopped when they are equal. At this point the controlling equation is:

(3) $R \text{ Sin } \theta \cos Y = R \cos 0 \sin Y$

When the above is true (comparison reached);

$$\theta = X$$

so at this point the multiplier registers contain a value of Y equal to θ (to a resolution of $\pm 0.1°$) which is presented on the front panel nixie readouts.

At this point the inputs to the two multipliers are reversed without distrubing the multiplicand (Y). Now the two multiplier outputs are:

$$\text{Cos Multiplier output} = R \cos \theta \cos Y$$

$$= R \cos \theta \cos \theta$$

$$= R \cos^2 \theta$$

$$\text{Sin Multiplier Output} = R \text{ Sin } \theta \text{ Sin } \theta$$

$$= R \text{ Sin}^2 \theta$$

These two multiplier outputs are now summed to yield:

(4) $\text{Sum} = R \cos^2 \theta + \text{Sin}^2 \theta$

$$= R$$

This value is then measured with an internal DVM and displayed on a second set of front panel nixie readouts. This completes the resolving of R and θ from the Cartesian Components.

MP MASTER
MA33503